TRS-80 T.M. MODEL II

TECHNICAL REFERENCE MANUAL

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Radio Shack®
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IMPORTANT NOTICE

This Technical Reference Manual is written for owners of the TRS-80 Model II Microcomputer who have a thorough understanding of electronics and computer circuitry. It is not written to the beginner's level of comprehension.

Radio Shack will not be liable for any damage caused, or alleged to be caused, by the customer or any other person using this technical manual to repair, modify, or alter the TRS-80 Model II Computer in any manner.

Many parts of the computer electronics are very sensitive and can be easily damaged by improper servicing. We strongly suggest that for proper servicing, the computer be returned to Radio Shack.

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3. The cost for the labor and parts required to return the Radio Shack computer equipment to its original manufacturer's specifications will be charged to the customer in addition to the normal repair charges.

An Overview

This Technical Reference Manual presents a comprehensive theory of operation for the CPU Module, the FDC, Video/Keyboard, Video Display, Disk Drives and the Power Supplies. There are also general checkout procedures to aid you the user in tracing problems down to a specific sub-assembly or P. C. Board — but no lower.

This Manual limits repair procedures to replacement of subassemblies only. A parts list containing part numbers for major subassemblies may be found at the end of the Troubleshooting and Replacement section. A detailed parts list for each subassembly may be found at the end of the section describing that particualr subassembly. Individual components may be ordered through your local Radio Shack store using the Radio Shack Part Number or the Manufacturer's Part Number if the Radio Shack Part Number is not available.

We have included in this Manual — for reference only — the Shugart Diskette Storage Drive Manual, 800/801 and the CDC Flexible Disk Drive Manual, 9404B. Data sheets on several of the Integrated Circuit chips used in this system are also included to provide the user with additional data concerning the operation of these devices.

To aid you in recognizing problem areas, you may purchase a Software Diagnostics Diskettè from your Computer Center or Radio Shack Store.

If you have any further problems with the TRS-80 Model II Microcomputer System, contact your Radio Shack Store or Computer Center.

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SECTION I

SYSTEM DESCRIPTION

A. INTRODUCTION

The TRS-80 Model II Microcomputer is a disk-based computer system consisting of three major components, the third of which is optional. They are: a Video Display Console with built-in Disk Drive, a separate Keyboard Unit and the optional Disk Expansion Unit.

Video Display Console

The Video Display console is made up of ten major subassemblies: (Refer to Figure 1.)

1. **Case:**

   The case subassembly has three major parts, the bottom tray, the top cover and the front bezel. These parts provide the attractive housing for the TRS-80 Model II. Care should be exercised during service operations so that the painted case parts are not marred or scratched.

2. **Chassis:**

   The metal chassis is mounted to the bottom tray of the case. The chassis has mounting provisions for the other subassemblies in the TRS-80 Model II.

3. **Power Supply:** (Refer to Figure 2.)

   The power supply subassembly in the TRS-80 Model II is an open frame, 150 watt, switching power supply. It has four outputs with the following ratings:

5	Volts	@	8.6	Amps
12	Volts	@	4.5	Amps
24	Volts	@	1.7	Amps
-12	Volts	@	0.2	Amps

   The power supply rectifies the AC line to DC, chops it at 20 kHz, then transforms the chopped DC to the required output voltages and finally rectifies the transformed output to low voltage isolated DC. Feedback loops are provided for voltage regulation and over current protection.

   The power supply may be jumper selected for either 95 to 135 VAC or 190 to 270 VAC. It will operate at either 50Hz or 60Hz input frequency.

   CAUTION

   This power supply must have a load present, i.e., the computer and CRT, or damaging oscillations may result.

   Never test the power supply without a suitable load. The minimum currents required by the power supply are:

5	Volts	@	2.15	Amps
12	Volts	@	1.25	Amps
24	Volts	@	0.00	Amps
-12	Volts	@	0.05	Amps

4. **Card Cage:**

   The card cage provides mechanical support for and electrical connections to the digital electronics boards. Up to eight boards can be accommodated in the card cage. The main component of the card cage subassembly is the "Motherboard". The Motherboard holds the eight 80 pin card edge connectors and has the printed wiring defining the TRS-80 Model II bus.

   As shipped from the factory, the cards should be in the following order: (slot one being the one closest to the power supply).

CPU	Slot 1
FDC	Slot 2
Memory	Slot 3
Video	Slot 4
Expansion Mem	Slot 5 (ie. the 32K memory add on board)

5. **CPU Card:**

   The CPU card in the TRS-80 Model II has several powerful features. The first of these is, of course, the CPU itself, a 4 MHz Z80A Microprocessor, running at its full rated speed.

   The bootstrap ROM on the CPU card provides the necessary instructions to the Microprocessor for the required initialization of the computer system on power-up or after a front panel reset. The ROM then "disappears", allowing the user to take full advantage of the memory space as RAM.

   The DMA (Direct Memory Access) circuit on the CPU board allows memory to peripheral or peripheral to memory data transfers without CPU intervention. This allows for a much greater program and I/O throughput. One of the most often used applications of the DMA is in data transfers to and from the Floppy Disk Controller. The dual serial interface is also on the CPU card. The baud rate is fully user programmable (refer to your Owner's Manual.

6. **Floppy Disk Controller Card:**

The floppy disk controller card provides all the circuitry necessary to read and write in both single density (FM) and double density (MFM) formats on an eight-inch floppy disk drive. The board uses an FD1791 floppy disk controller chip to generate the proper write signals. The read signals from the drive are passed through a phase-locked loop data separator before going on to the FD1791 to insure high reliability reads.

CAUTION

The phase-locked loop is factory adjusted for optimum performance. Do not adjust any of the potentiometers on the FDC board).

The parallel printer interface is also on the floppy disk controller card.

7. **Memory Card:**

The memory card in the TRS-80 Model II uses 16K dynamic RAMs to give either 32K bytes or 64K bytes of read/write memory. The necessary refresh signals for the memory come from the CPU board.

8. **Video Card:**

The video card supports both 80 character and 40 character lines, with 24 lines displayed. The character set includes upper and lower case alphabetic and numeric symbols (↑ . . . #, etc.) and a set of forms drawing characters. Reverse video can be selected on a character-by-character basis.

The heart of the video controller is a 6845 CRT controller chip, which is software programmable for various formats.

The video card also contains the logic for the keyboard interface. This serial handshake interface receives data and clock signals from the keyboard and issues an interrupt when the entire character has been received.

9. **Video Monitor (CRT):**

The 12 inch CRT (Cathode Ray Tube) and associated electronics form the video monitor for the TRS-80 Model II. This subassembly receives video, horizontal drive, and vertical drive signals from the video card and +12 volts from the power supply. The CRT's high resolution complements the upper/lower case character set of the video card.

10. **Floppy Disk Drive:**

The floppy disk drive is a standard eight inch drive capable of supporting both single and double density recording formats. All of the disk drive control signals come from the floppy disk controller card. The drive contains two motors; one rotates the media at a constant speed while the other positions the read/write head over one of the 77 tracks. Electronics on the disk drive convert digital signals into read/write head signals and vice-versa.

NOTE

Models for overseas shipment may be configured with an AC Moter for the line voltage available in that country and may be fitted with a different drive pulley for 50 Hz line frequency.

A detailed description and theory of operation of each subassembly, with the exception of the Case and Chassis, may be found in later sections of this manual.

Keyboard Unit

The keyboard of the TRS-80 Model II is a 76-key microcomputer controlled capacitive keyboard. The microcomputer and its associated electronics scans the key matrix, converts switch closures to an eight bit digital code and transmits it serially to the keyboard interface on the video card. The keyboard is connected to the main console via a cable from the front bezel of the computer.

Peripheral Interfaces

There are four interface connections on back of the Video Display Console:

1. Two serial (RS-232-C) Input/Output (I/O) channels.
2. A parallel I/O channel, e.g. for connection to TRS-80 standard parallel-interface line printers.
3. Floppy Disk I/O channel for connection of the Model II Disk Expansion Unit.

The Video Display Console also provides connectors and slots for future expansion. (See Operator's Manual).

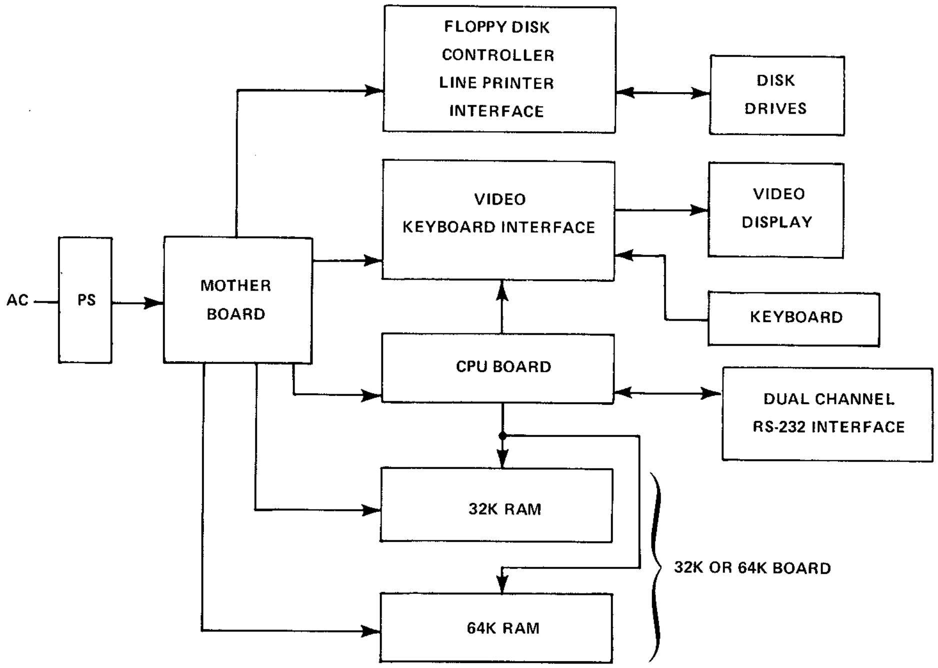


Figure 1. TRS-80 Model II Block Diagram

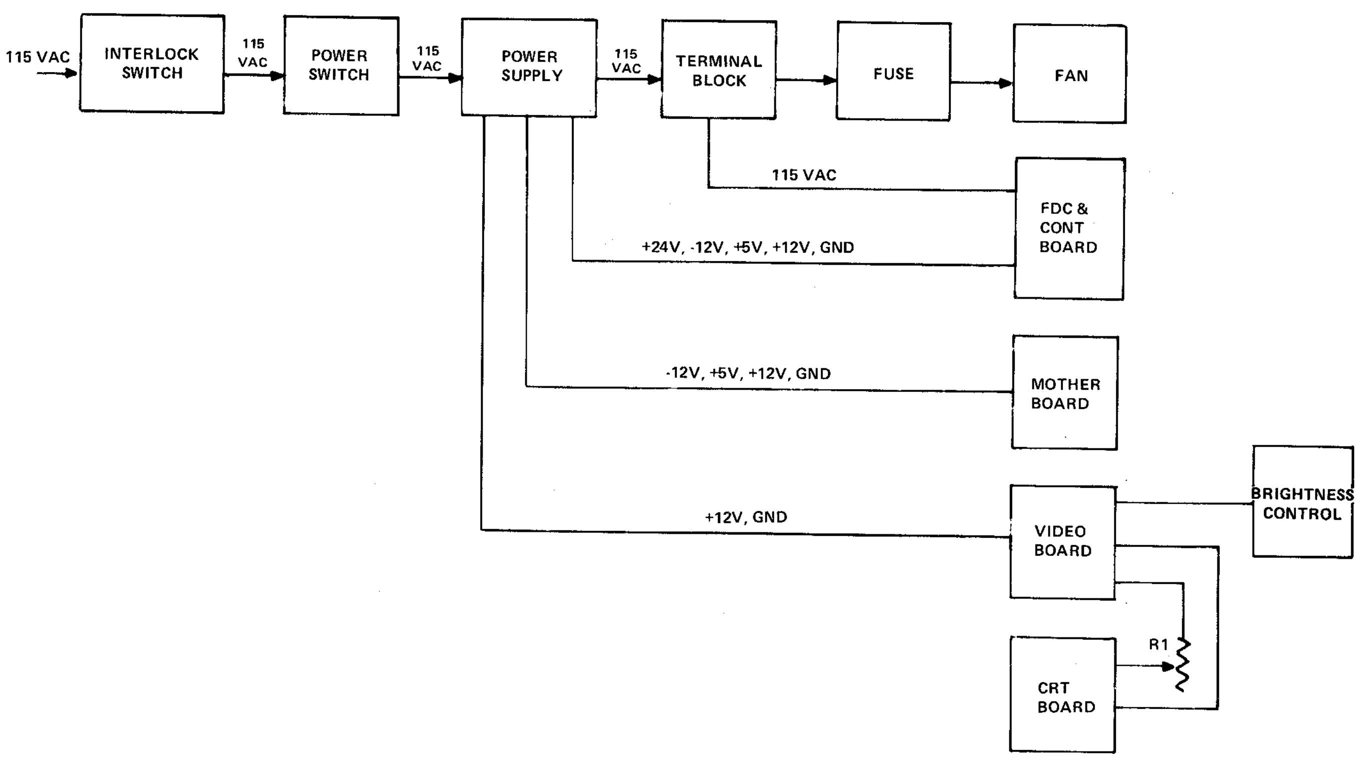


Figure 2. TRS-80 Model II Power Distribution Block Diagram

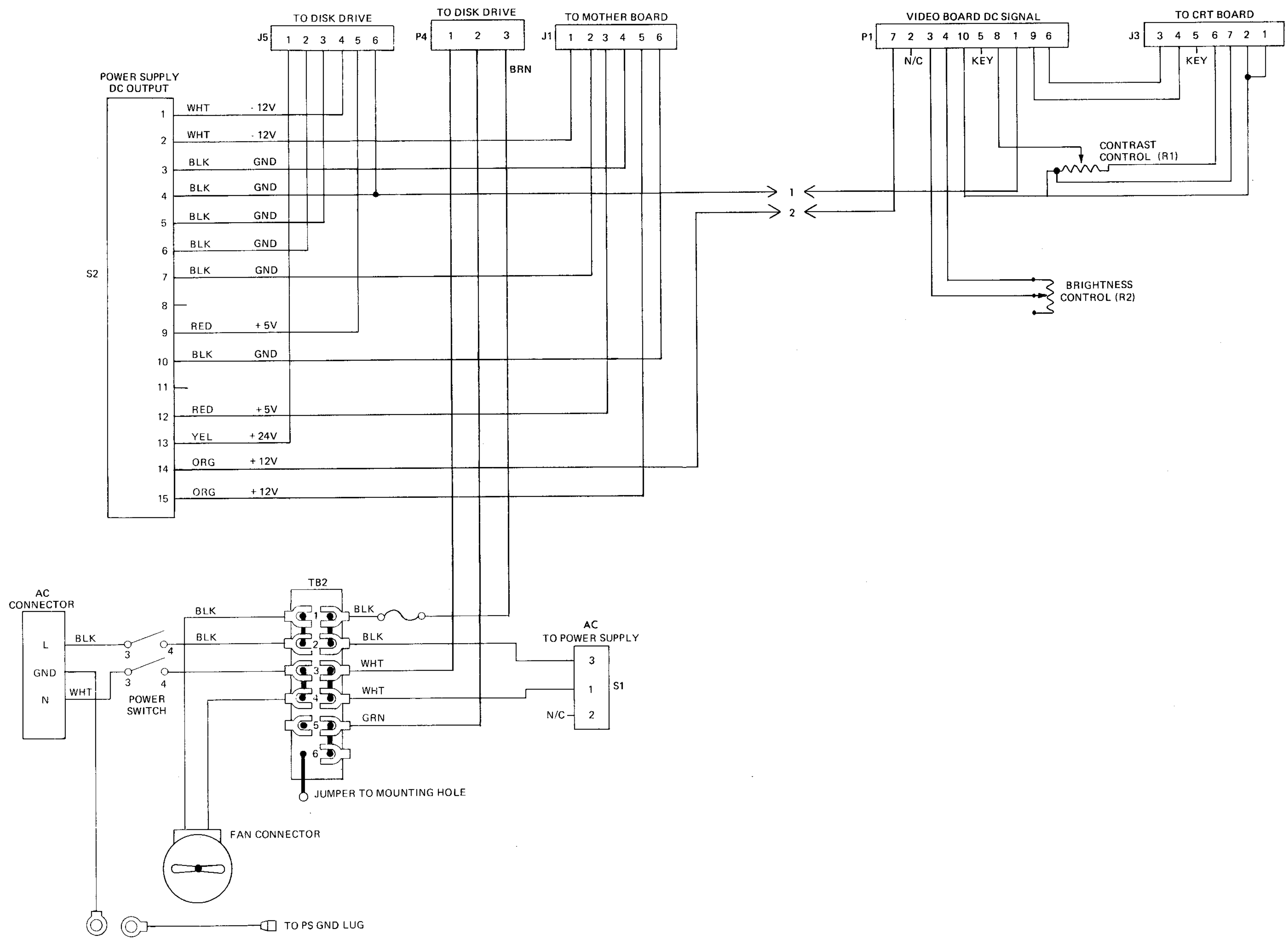


Figure 3. TRS-80 Model II Power Distribution Schematic

SECTION II

TROUBLESHOOTING/REPLACEMENT

A. TROUBLESHOOTING PROCEDURE

General

This section of the manual will guide service personnel through the system checkout procedure. The troubleshooting steps are organized in a flowchart manner. Following these steps will guide you to the possible failing board or boards.

Connect the power cord and keyboard as described in the Operator's Manual.

Remove the top cover of the display console by removing the two screws at the rear of the unit. Carefully set the top cover aside to prevent accidental scratching. If the unit has an interlock switch, enable the test mode by pulling up on the interlock switch plunger.

At this point, there should be no diskette in the drive, and the disk terminator should be installed as described in the Operator's Manual.

Synopsis of Power-On Diagnostics

When the power switch on the TRS-80 Model II is raised to the "ON" position, the Z80 microprocessor automatically starts executing the program in the bootstrap ROM on the CPU board. The program performs the following functions in order:

1. The initialization parameters are sent to the CRT controller and the screen memory is set to the value ØAØH. This causes the CRT to come on with a solid white screen.

2. The ROM checksum is verified to assure that the ROM is present and functioning properly. If the checksum indicates that the ROM data is bad, "CK ERROR" will be outputted to the CRT and the computer will halt.

3. A CPU test program is run to verify proper data transfers between registers in the Z80 CPU. Any failure of this test will cause "Z8 ERROR" to be output to the CRT and the computer will halt.

4. The RAM memory from 1ØØØH to 7FFFH is then tested with a simple read-complement-write-compare-complement-write routine. Any faulty memory locations in this 28K byte range will cause "MF ERROR" to be output to the CRT and the computer will halt.

5. The keyboard will be "flushed" of any characters input up until this time.

6. The message "INSERT DISKETTE" is displayed on the CRT.

Bootstrap Sequence

7. Wait until diskette is inserted and door is closed.

8. Screen is cleared to spaces (all black).

9. Track Ø seek command is sent to floppy disk controller.

10. Wait three seconds and check disk status.

11. "DC ERROR" if floppy disk controller is still busy or seek error is indicated or drive not restored to track Ø.

12. "DØ ERROR" if drive Ø indicates not ready.

13. "SC ERROR" if there is a CRC error in the track ID field.

14. Read track Ø into RAM.

15. "TK ERROR" if program not found on track Ø.

16. "SC ERROR" if there is a CRC error in the record ID.

17. "LD ERROR" if a lost data error occurs.

18. "RS ERROR" if the data loaded in is not in Radio Shack boot record format.

19. Call system diagnostic routine.

20. Jump to TRSDOS.

Detailed Troubleshooting Instructions

1. Turn on the Model II Computer by raising the power switch to "ON". Wait a few seconds for the CRT to warm up. Adjust brightness and contrast controls at the front of the console. If the video display comes on, go to 10. If not, go to 2.

   NOTE: For overseas models configured for 50 Hz operation, the "HERZ50" programs on the TRSDOS diskette must be called to prevent "jittering" of the video display and to provide accuracy of the real time clock.

2. If the pilot light is on, go to 4. If the pilot light/reset switch connector is seated correctly on the CPU board, go to 3. If not, reposition the connector and go to 2.

3. Check for +5 volts on one of the P.C. boards. If this is not in the range from 4.8 to 5.2 volts, go to 5. If the voltage is incorrect, the LED must be burned out. Replace and go to 1.

4. Check the filament of the CRT. If it is lit, go to 7. If it is not:

   Check the +12 volt supply at the CRT electronics board (pin 1 is ground, pin 7 is +12V).

   If +12 volts is present, go to 6.

5. Switch off power. Check the power supply fuse and replace if necessary. Check for shorts across the power supplies. If shorts are found, remove cards from card cage until the shorts disappear, then replace the offending card. Reassemble and go to 1.

   Otherwise, power supply may have malfunctioned. Remove and replace the power supply. Go to 1.

6. CRT has burned out filament. Replace and go to 1. (Refer to Section VII for installation procedures.)

7. Look at pins 6 and 9 on the CRT Monitor P.C. Board and compare the signals to Figure 1. If the respective signals are the same, go to 9. If not:

   Turn off power. Swap video board with a known good one. Try again. If video display comes on, go to 10.

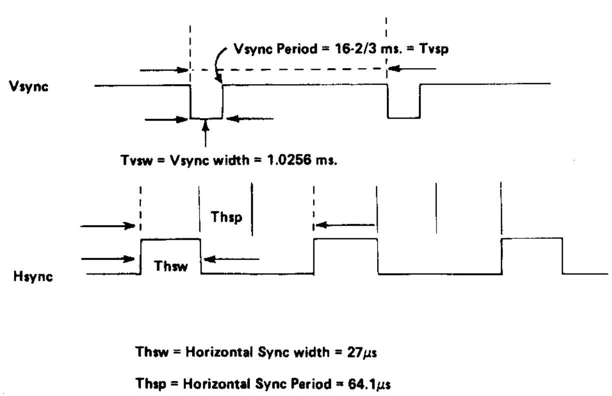


Figure 1. Sync Signals

8. If unable to return the computer to an operational condition, it should be returned to Radio Shack for servicing by factory trained technicians.

9. Replace CRT Electronics and try again. If video display comes on, go to 10. If not: go to 8.

10. If the CRT displays a white screen with "INSERT DISKETTE" in the center, proceed to **Software Diagnostics** below. If not:

    If CRT displays white screen with some other message, go to 11.

    Turn off power and replace video card. If that cures the problem, go to 10.

    Turn off power and reinsert original video card. Replace CPU board. If that cures problem, go to 10.

    Turn off power and reinsert original CPU card. Go to 8.

11. If message says "CK ERROR", there is a ROM checksum error. This means the bootstrap ROM does not check out good. Either replace ROM or CPU board and go to 1.

    If message says "Z8 ERROR", there is a CPU error. Either replace the Z80 CPU on the CPU board or replace the entire CPU board and go to 1.

    If message says "MF ERROR", a RAM error has been detected in the lower 32K bytes. Replace the memory card and go to 1.

Software Diagnostics

Further testing can be accomplished at this time using the Diagnostic Diskette and the TRS-80 Model II Troubleshooting Manual. The memory, line printer, Floppy Disk and video alignment are some of the checks that can be made with these diagnostic "tools".

The Diagnostic Diskette (Part Number AXX2012) can be purchased through your Computer Center or Radio Shack store.

B. REPLACEMENT PROCEDURES

Replacement procedures contained in this manual are limited to system disassembly, removal and replacement of subassemblies and system assembly.

There are potentially hazardous areas inside the case, so use caution during disassembly and be sure to read and observe the warning and caution notes.

Disconnect all external cables from the rear connector panel before beginning repair.

System Disassembly

1. **Case:**

   a. Remove the two machine screws from the back of the case.

   b. Lift up on the rear of the top case and angle it toward the front panel; then lift the top case away from the bottom.

   c. Remove the two screws from the video display mounting bracket and bezel.

   d. Remove the screw that secures the mounting bracket on top of the disk drive to the bezel (inside of front panel).

   e. Pull out the keyboard cable only as far as necessary to allow the front panel to lay flat (face down).

   f. Pull the front panel forward to clear the chassis and lay it face down.

2. **Chassis:**

   a. Remove five #8 screws, flat washers and lock washers from locations illustrated. Notice that one of the screws is used to help mount the power supply.

   b. Lift up chassis slightly (to clear ribs in the bottom case) and slide it forward.

   c. Remove screws holding the AC power connector to the connector panel and remove the connector from the panel.

   d. Disconnect two wires from the fuseholder.

   e. Disconnect all I/O cables from disk drive, CPU card and FDC card.

   f. Remove chassis from the bottom case.

3. **Power Supply:**

WARNING

If the power supply is faulty, the large heat sink may have a potential of 330 volts above line common. Use extreme caution when handling the power supply.

   a. Remove the three-wire AC plug and the thirteen-wire DC plug from the power supply PCB.

   b. Remove two #8 thread forming screws from the power supply mounting bracket.

   c. Tilt the power supply toward the outside of the chassis and remove four screws, nuts and spacers that mount the video board to the power supply mounting bracket.

   d. Remove five screws, nuts, flat washers and spacers that secure the power supply to its mounting bracket.

   e. Remove the power supply from the chassis.

4. **Card Cage:**

   a. If not previously done, disconnect the signal and control cables from the video/keyboard card and I/O cables from the floppy disk controller and CPU cards.

   b. Disconnect the DC cable on the lower right front of the mother board.

   c. Remove four #8 thread forming screws from the card cage mounting bracket.

   d. Remove card cage from the chassis.

5. **Removal of Cards from Card Cage:**

   a. Remove two thread forming screws that connect the PCB stabilizer to the card cage mounting brackets and remove the stabilizer.

   b. Notice the location of the CPU, FDC, video/keyboard and memory cards. Ensure that the replacement cards are inserted in the same locations.

   c. Remove and replace cards as necessary for repair.

   d. Remove six screws, nuts and flat washers that mount the mother board to its mounting brackets and remove the mother board.

6. Video Display (CRT) and Video Board:

> **CAUTION**
>
> The CRT and video board are matched sets. Do not remove and replace individual pieces. Remove one matched set and replace with another matched set.

a. If the video board is not free from the power supply mounting bracket, perform the steps for removal of the power supply down to removal of the video board.

b. Disconnect four color coded wires with spade lugs from the CRT yoke.

c. Disconnect the connector on the rear of the CRT neck.

> **WARNING**
>
> There may be a high voltage charge on the high voltage anode. To discharge, connect one end of a wire to a known good ground and connect the other end of the wire to the blade of a common screwdriver. Insert the screwdriver blade under the suction cup and touch it to the clip holding the wire to the CRT.

d. Insert a common screwdriver under the rubber grommet on the high-voltage anode wire on the side of the CRT. Use the screwdriver to compress the clip holding the wire to the tube and pull the wire free.

e. Remove the upper right and lower left screws, nuts and washers from the video display mounting bracket.

> **CAUTION**
>
> If dropped, the CRT will implode. To avoid this kind of accident, support the CRT while performing the next step.

f. Remove the lower right and upper left screws, nuts and washers from the video display mounting bracket.

g. Lift the CRT and PCB out of the chassis.

7. Disk Drive

a. Disconnect two power connectors from the disk drive PCB.

b. Disconnect the large (50 pin) card edge connector from the disk drive PCB.

c. Remove four screws from the disk drive mounting bracket.

d. Lift the drive and mounting brackets out of the chassis.

e. Lay the drive on its side (PCB up) and remove two screws from the bottom of the mounting bracket.

f. Separate the drive from the bracket.

8. Fan

NOTE: The following steps can only be performed with the chassis removed from the case.

a. Position the chassis so that the four nuts on the bottom of the chassis are accessible.

b. Disconnect the power cable on the fan.

c. Secure the screw heads while removing the nuts from the bottom of the chassis and remove four nuts.

d. Raise the fan away from the chassis to provide clearance for the screws while removing the fan.

9. Keyboard (See Figure 2):

a. Disconnect the keyboard external cable from the keyboard (DIN plug.)

b. Place the keyboard with keys down on a soft surface.

c. Remove four thread forming screws and two machine screws.

d. Place the keyboard with keys up and remove the bezel.

e. Disconnect the five-pin connector at J1 on the PCB.

f. Lift the keyboard with PCB out of the case.

Reassembly

1. Keyboard:

Reassemble the keyboard in reverse order of disassembly.

2. Fan:

a. When installing a new fan, insert the screws into the screw holes before positioning the fan.

b. Ensure that the fan is oriented so that air will flow in from the bottom and out through the top and so that the power connector is accessible.

> **CAUTION**
>
> Do not put stress on the fan mounting ears. Tighten the screws and nuts only enough to secure the fan to the chassis.

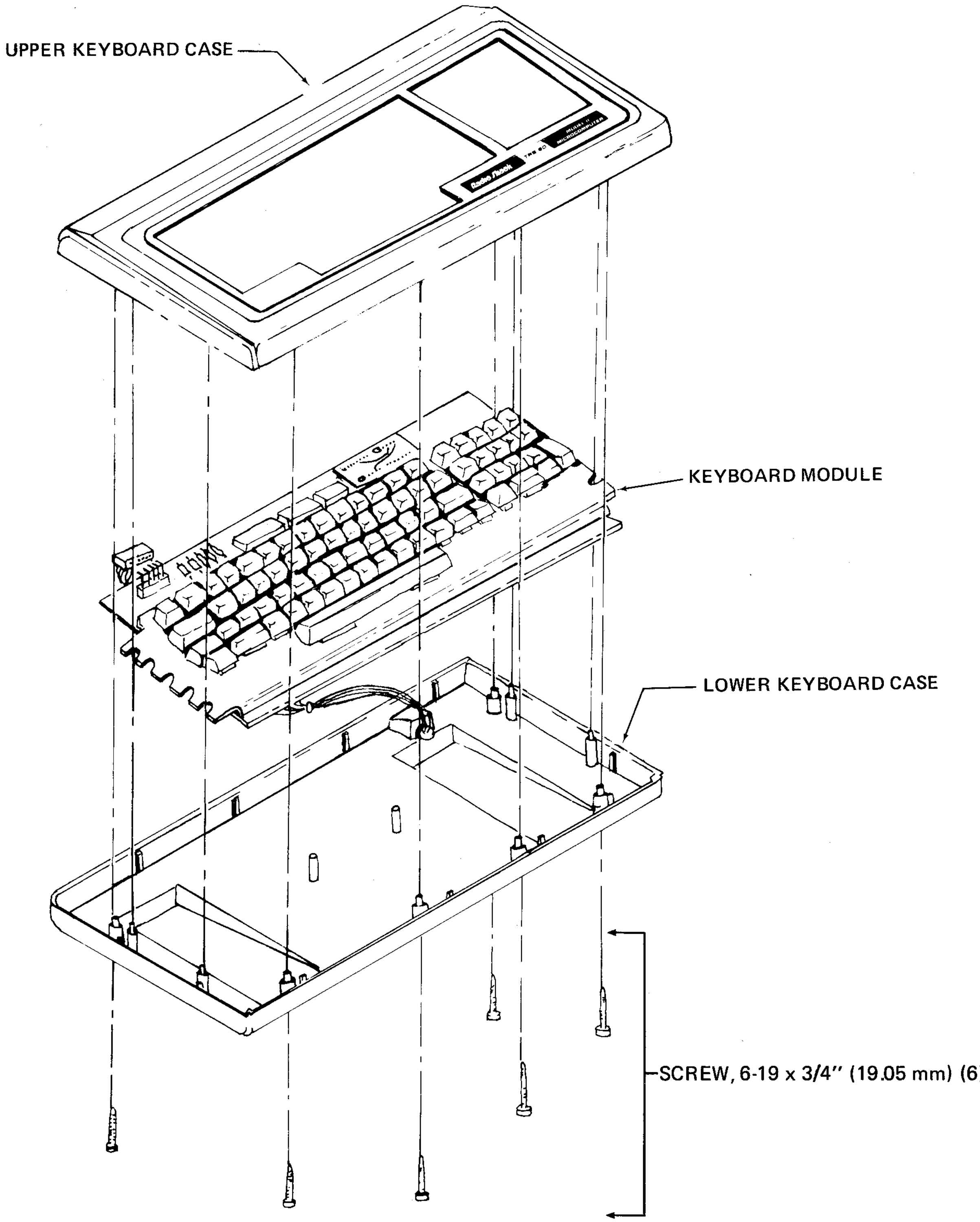


Figure 2. Disassembly of Keyboard

c. Position the chassis so that the fan mounting screws are accessible from the bottom of the chassis.

d. Secure the screw heads while installing the nuts.

e. Tighten the nuts only enough to ensure that the fan is secure.

3. **Disk Drive:**

   a. Lay the disk drive on its side (PCB up) and position its chassis mounting bracket (wide end forward) to align holes in bracket with the holes in the drive base plate.

   b. Install two screws that secure the drive to the mounting bracket.

   c. Place the drive with mounting bracket into the chassis and align the screw holes in the bracket and in the chassis.

   d. Install four screws loosely so that the drive's position can be properly adjusted. Then tighten the screws that secure the bracket to the chassis.

   e. Install two power connectors and the card edge connector on the drive.

4. **Video Display (CRT) and Video Board**

   a. Position the CRT and align its mounting holes with its mounting bracket.

   b. Install the upper left and lower right screws and mounting hardware.

   c. Install the lower left and upper right screws and mounting hardware.

   d. Position the CRT matched video board inside of the chassis.

   e. Install the plug on the rear of the CRT neck.

   f. Install the four color coded wires with spade lugs to their associated terminals (as determined by a colored dot on the yoke near each terminal).

   g. The video board will be installed on the power supply mounting bracket, (see the procedures for installation of the power supply).

5. **Card Cage:**

   a. Align the mother board mounting holes with the holes in the left and right PCB mounting brackets. (The left bracket has a left 90° bend at the rear and the right bracket has a right 90° bend at the rear).

   b. Install six screws, nuts and flat washers that secure the mother board to the brackets.

   c. Install the CPU, FDC, video/keyboard and memory cards to the mother board. Be sure of proper orientation in the card cage.

   d. Align the holes in the PCB stabilizer with the holes in the left and right PCB bracket and install two thread forming screws.

   e. Position the card cage inside of the chassis and align the holes in the brackets with the holes in the chassis.

   f. Install four screws that secure the card cage to the chassis.

   g. Connect the DC cables to the connector on the lower right front of the mother board.

   h. Connect the I/O cables to the FDC and CPU cards and connect the control cables to the video/keyboard card.

6. **Power Supply:**

   a. Align the power supply mounting holes with the holes in its bracket mounting plate.

   b. Individually, position five spacers to align with the mounting holes between the power supply board and its mounting plate.

   c. Install five screws, nuts and flat washers that secure the power supply to the bracket.

   d. Position the power supply in the chassis and tilt it toward the outside of the chassis.

   e. Align the video board mounting holes with its mounting holes on the power supply bracket mounting plate.

   f. Position four spacers to align with the mounting holes.

   g. Install four screws, nuts and flat washers that secure the video board to the bracket.

   h. Position the holes in the mounting bracket to the holes in the chassis and install two thread forming screws that secure the bracket to the chassis.

7. **Chassis:**

   a. Position the chassis inside the bottom case so that the two wires can be connected to the terminals on the fuse holder and the AC power input connector can be installed on the connector panel.

   b. Install the two wires to the fuse holder.

   c. Install two screws that secure the AC power input connector to the connector panel.

d. Lift up the chassis (to clear the ribs on the case bottom) and position it so that its mounting holes align with those in the case.

e. Install five screws, flat washers and lockwashers that secure the chassis to the bottom case.

8. Case:

a. Position the front panel (bezel) on the chassis.

b. Install one screw that secures the bezel to the top bracket on the disk drive.

c. Install the two screws that secure the bezel to the video display mounting bracket.

d. Position the top case at the lip of the bottom case and angle it downward (toward the back) until the top case is properly seated.

e. Install two machine screws that secure the top case to the bottom case.

REPLACEMENT PARTS LIST (Subassemblies)

Description	Manufacturer's Part Number	Radio Shack Part Number
CPU Board	8893405	AXX0501
CRT (with Video Board)	8709043	AXX8000
Disk Drive, SA800	8709042	AXX5002
Disk Drive, SA800 PCB	———	AXX0308
FDC Board	8893425	AXX0505
Keyboard Module	8790504	AXX0204
Memory Board, 32K	8893410	AXX0502
Memory Board, 64K	8893415	AXX0503
Mother Board Assembly	8893430	AXX0500
Power Supply, AA11080	8790010	AXX6003
Video Generator Board	8893420	AXX0504

SECTION III

CPU MODULE

A. FUNCTIONAL SPECIFICATIONS

The TRS-80 MODEL II CPU Board provides the following hardware resources for the system:

1. Performs data processing activities.
   a. Supports DMA operations, both on the CPU Board or on an external system board.
   b. Supports mode 2 vectored interrupts.

2. Provides primary DMA channel.

3. Provides dual serial I/O channels.
   a. RS-232C standard signals.
   b. Asynchronous and synchronous schemes supported. Bisync, SDLC, and HDLC protocols are supported.

4. Provides timing signals needed by the system.
   a. 2 or 4MHz system clock option.
   b. Programmable serial I/O baud rate clocks.
   c. 8MHz clock for write precomp on FDC Board.
   d. Real time clock
   e. Control signals for system boards.
   f. Flexible on and off board wait state generation.

5. System bootstrap firmware (2716 compatible).
   a. Resides in low memory if enabled (location ØØØØH to ØFFFH).
   b. Software switchable enable.
   c. Self test diagnostic software included.

6. Power on and manual reset logic.

The major components employed include the following:

1. ZSØA CPU Chip (Central Processing Unit)

2. Z8ØA DMA Chip (Direct Memory Access)

3. Z8ØA SIO Chip (Serial Input/Output)

4. Z8ØA CTC Chip (Counter Timer Circuit)

5. 2716 Compatible ROM (Read Only Memory)

B. THEORY OF OPERATION

Decoding Logic

The peripheral devices on the CPU Board are I/O mapped, with the exception of the BOOT ROM. The port addresses used are FØH through F9H. Port mapped devices use the lower eight address bits only to specify which port is being addressed. The upper eight address bits are ignored completely and are not relevant to port mapped devices. Three other signals (WR*, RD*, and IOCYC*) are used by port mapped devices to determine whether an input or output operation is to occur. If RD* and IOCYC* are both low, this condition specifies that an input operation is in progress. If WR* and IOCYC* are both low, this condition specifies that an output operation to the addressed port is in progress.

Sheet 3 of the CPU schematic should now be referred to. U36, U37, and one half of U38 are used to decode the I/O addresses required for the CPU Board. U36 is an open collector output BCD to decimal decoder which brings one of its outputs low, dependent upon the binary combination presented to the inputs A through D. These outputs become the chip enables for the peripheral devices used.

One half of U37 (4-input NAND gate) is used to detect when any of the ports used are being addressed. This output is inverted and presented to pin 1 of U16. One half of U5 and one sixth of U14 detect an input or output operation in progress, based on the state of RD*, WR*, or IORQ*.

This output is presented to pin 2 of U16. A low is produced at pin 3 of U16 when any of the valid ports are addressed and an input or output operation is in progress.

This output is combined at pin 13 of U14 with the signal labeled RDROM* at pin 12 of U14 to produce a low going strobe labeled SELECT*. RDROM* goes low if a Read from the BOOT ROM is in progress.

Therefore, if SELECT* is low, this indicates that an input or output operation to the valid ports is occurring or that a Read from the BOOT ROM is in progress. SELECT* is gated to pin 43 of the system bus via a tri-state buffer (1/6 of U39). This signal may be monitored with a scope while executing a diagnostic program, to verify proper operation of the decoding logic.

The BOOT ROM is a memory mapped device which, when enabled, occupies the lower 4K of the system address space (addresses ØØØØH through ØFFFH). Half of U38 and one fourth of U5 decode the upper address bits (A12 through A15) to detect an address within this range. The output produced from this logic (U5 pin 11) is gated with ROM*/RAM to produce a low at U5 pin 8 if the BOOT ROM is enabled. One half of U16 combines the output of A11 and its logical inverse to produce two ROM chip enables (ROMØCE* and ROM1CE*). ROMØCE* is active for the address range ØØØØH through Ø7FFH, while ROM1CE* is active for addresses Ø8ØØH through ØFFFH. (ROM1CE* is not currently used and is not connected to any other logic). RD* and MREQ* are decoded by one sixth of U3 to detect a memory read in progress. When this signal (U3, pin 8 and ROMØCE*) is low, the BOOT ROM is allowed to gate out the data pattern corresponding to the byte being addressed to the internal data bus.

IORQ* and WR* are decoded by one sixth of U5 to produce the signal labeled OUT* (U5 pin 3). This output, when combined with the signal F9* (U36 pin 11) by one fourth of U3, produces a low going strobe at pin 11 of U3. This signal indicates that an output operation is occurring to port F9H. The rising edge of this signal latches the state of DØ into one fourth of U13, "D" Flip-Flop (see sheet 2 of CPU schematics). The Q* output of this Flip-Flop is fed back to U5 pin 9 and enables or disables the BOOT ROM. An output operation to port F9H with DØ set, enables the BOOT ROM. If DØ is reset the BOOT ROM will be disabled. The set input of this Flip-Flop is tied to RESET. Therefore power on or manual reset will automatically enable the BOOT ROM. Below is a table which outlines the port address allocation for the CPU Board.

PORT ADDRESS ALLOCATION

Port No.	Allocation	Function
FØH	CTC	Channel Ø
F1H	CTC	Channel 1
F2H	CTC	Channel 2
F3H	CTC	Channel 3
F4H	SIO A	Channel A data
F5H	SIO B	Channel B data
F6H	SIO A	Channel A Command/Status
F7H	SIO B	Channel B Command/Status
F8H	DMA	DMA Command/Status
F9H	ROM ENABLE LATCH	ENABLES/DISABLES ROM

Bus Steering Logic

The system data bus is a bidirectional path, which means that data may be driven to the system bus or received from the system bus. Outputs to external ports or writes to the system memory require that data be driven to the system bus. Inputs from external ports, interrupt acknowledges from external devices, or reads from system memory other than the BOOT ROM, require that the data is received from the system bus. This problem is somewhat complicated by the fact that data must not be received from the system bus when an input, interrupt acknowledge from an external device, or a Read operation is in progress from CPU Board resident devices.

U31 and U32 are the devices which switch the data to and from the system bus. One third of U22 is used to detect a READ, interrupt acknowledge or input cycle in progress. U22 pin 12 goes low if any of these operations are occurring. Half of U13 and one fourth of U21, detect the presence as a pending interrupt from a device on the CPU Board. An interrupt request from one of the devices on the CPU Board will force U13 pin 4 low, which in turn forces U13 pin 6 low. This output is combined with INTAK* at pins 1 and 2 of U21 to produce the signal LOCAL INT PENDING. This signal when low, prevents U22 pin 8 from going low.

This indicates that an interrupt from one of the devices on the CPU Board is being acknowledged and that the data bus receivers should not be enabled. U22 pin 9 (SELECT*) performs the same function if any of the devices on the CPU Board are selected by a memory read or an I/O operation. If pins 10 and 9 of U22 are both high, pin 11 of U22 when high will force pin 8 of U22 low. This enables the data receivers to gate data onto the CPU data bus for either a memory read, input operation, or an interrupt acknowlege.

The bus steering logic also allows an external DMA operation to occur by disabling the data bus drivers and the address and control line buffers when this condition is detected. BUSRQ* and BAO (inputs to U3) indicate this condition when both are low. U3 pin 6 (DMA EXT*) is the corresponding output produced. If DMA EXT* is active (low) or U4 pin 9 is low, then pin 8 of U4 goes low, disabling the data bus drivers.

Wait State Generation Logic

The memory access time requirements are most severe during an M1 cycle instruction fetch. All other memory accesses have an additional one half clock cycle to be completed. The TRS-80 Model II system uses 2ØØns access time RAMS. One wait state must be inserted on M1 cycle instruction fetches when using this speed memory. The BOOT ROM is either a 2716 EPROM or a compatible mask ROM. Both of these parts are at best 300ns access time devices, which require one wait state per memory access if the BOOT ROM is enabled. U25 and U26 along with some associated gating, provide the wait state generation. Provisions have also been made for off board wait state generation. This feature is provided for external system boards which require non-standard timing for one reason or another.

Manual and Power ON Reset Logic

The Z8Ø-CPU has the characteristic that if the RESET* input goes low during T3 of an M1* cycle, the MREQ* signal will go to an indeterminate state for one T state approximately 1Ø T states later. This action could cause an aborted or short access of the dynamic RAM which could cause destruction of data present in the RAM. To avoid this problem, the falling edge of the RESET input must be

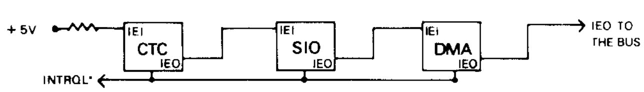
synchronized with the falling edge of M1*. One half of U28 and U27 perform this sychronization as well as provide a one-shot to limit the duration of the CPU RESET pulse. The one-shot duration is approximately 7Øns per switch depression, and is required to avoid suspending CPU refresh of dynamic memory for a period long enough to destroy RAM contents. Without the one-shot this could occur if the reset switch were held closed for a long period. The connector J2 connects the reset switch to this logic and also provides the current limited +5 volts for the "Power-On" indicator on the front panel.

System Clock Generation Logic

The heart of the clock generation logic is an 8 MHz crystal oscillator formed by Y1, C21, R23, R24, and three 74LS74 Flip-Flops (page 1 of the CPU schematics). The output of U29, pin 8 should be an 8 MHz square wave. The 8 MHz signal is divided down by one half of U28 and U2 to produce the 4 MHz, 2 MHz, and 1 MHz clocks needed by the system. The 8 MHz signal is buffered by one fourth of U30 and fed directly to pin 46 of the system bus. This clock is utilized by the write compensation circuitry of the FDC Board. A jumper option is provided to select either a 4 MHz or 2 MHz main system clock for the Z80 family parts. This output is divided by 2, to provide the clock inputs for the Z80-CTC when operating in the counter mode. Normal system operation requires that the main system clock run at 4 MHz and should be used at 2 MHz only under unusual circumstances. The output of U28 pin 9 (main system clock) is conditioned by the clock buffer circuitry implemented with Q1, C3, R2, R3, R4, and a 74S04 inverter. The clock buffer circuitry insures fast rise and fall times and close to 5 volts peak to peak amplitude transitions. These clock characteristics are important to the Z80A family of components when operating at maximum frequency (4 MHz).

Interrupt Priority Logic

The Z8Ø interrupt structure allows up to four Z8Ø family parts to be connected in a daisy chain fashion without any additional logic. Priority is set by the location of the device in a daisy chain configuration with each device tied to the INTRQL* line. The diagram below illustrates the relative priority of the devices on the CPU Board.



The IEI of the CTC is tied to +5 volts to indicate that it has the highest priority. The second highest priority device is the SIO with its IEI tied to the IEO of the CTC. The IEO of the SIO is tied to the IEI of the DMA. The IEO of the DMA is routed to the system bus where it is tied to the IEI of the next physical board in the system (FDC Board). The priority string insures that a device with higher priority will be serviced before a lower priority device when two or more INTRQL* requests occur at the same time. For a device to have priority, its IEI must be high. When a device needs service, it will prevent down stream devices from interrupting by pulling low on its IEO line. The next device in the chain, sensing a low at the IEI input, will pass this priority signal on to the next device by pulling low on its IEO line.

This priority scheme works fine as long as no more than four Z8Ø family devices are connected to the chain. If more than four devices are used, the delays through each MOS part get excessive and not enough time will be allowed to resolve interrupt contention. The Model II system currently uses four Z8Ø family parts in the daisy chain. To allow for expansion of the system, a carry look ahead scheme was employed using U23 (74S182) and four 74S04 inverters. This scheme anticipates IEO low condition at any of the three devices on the CPU Board and generates a look-ahead signal to the propagate output (U23 pin 7). This signal is inverted and fed to IEO (pin 14) of the system bus. This signal when low, prevents downstream devices from generating an interrupt and results in a 25ns maximum ripple time for any IEO to propagate out for the devices on the CPU Board. This allows up to four more family devices (eight total) to be used in the system without additional logic.

EIA Buffers

The logic internal to the CPU Board (SIO inputs and outputs in this discussion) operate with TTL logic levels (3.5V or more = Logic 1, and Ø.8V or less = Logic Ø). The logic convention used for interfacing two RS-232-C devices is EIA levels (-3V or less = logic 1, +3V or more = Logic Ø). The logic levels must therefore be converted from one convention to the other when interfacing to an external device. U10, U9, and U8 provide the EIA to TTL conversion while U7 and U6 provide the TTL to EIA conversion.

CONNECTOR J1 SIGNAL DESCRIPTIONS

PIN	SIGNAL DESCRIPTION
1	Power Ground
2	Not Connected
3	Transmit Data Channel A
4	Transmit S.E.T.
5	Received Data Channel A
6	Not Connected
7	Request to Send Channel A
8	Receiver Clock Channel A
9	Clear to Send Channel A
10	Not Connected
11	Data Set Ready Channel A
12	Not Connected
13	Power Ground
14	Data Terminal Ready Channel A
15	Carrier Detect Channel A
16-21	Not Connected
22	Transmit Clock Channel A
23	Not Connected
24	Not Connected
25	Not Connected
26	Power Ground
27	Not Connected
28	Transmit Data Channel B
29	Not Connected
30	Received Data Channel B
31	Not Connected
32	Request to Send Channel B
33	Receiver/Transmitter Clock Channel B
34	Clear to Send Channel B
35	Data Set Ready Channel B
36	Not Connected
37	Not Connected
38	Power Ground
39	Data Terminal Ready Channel B
40	Carrier Detect Channel B

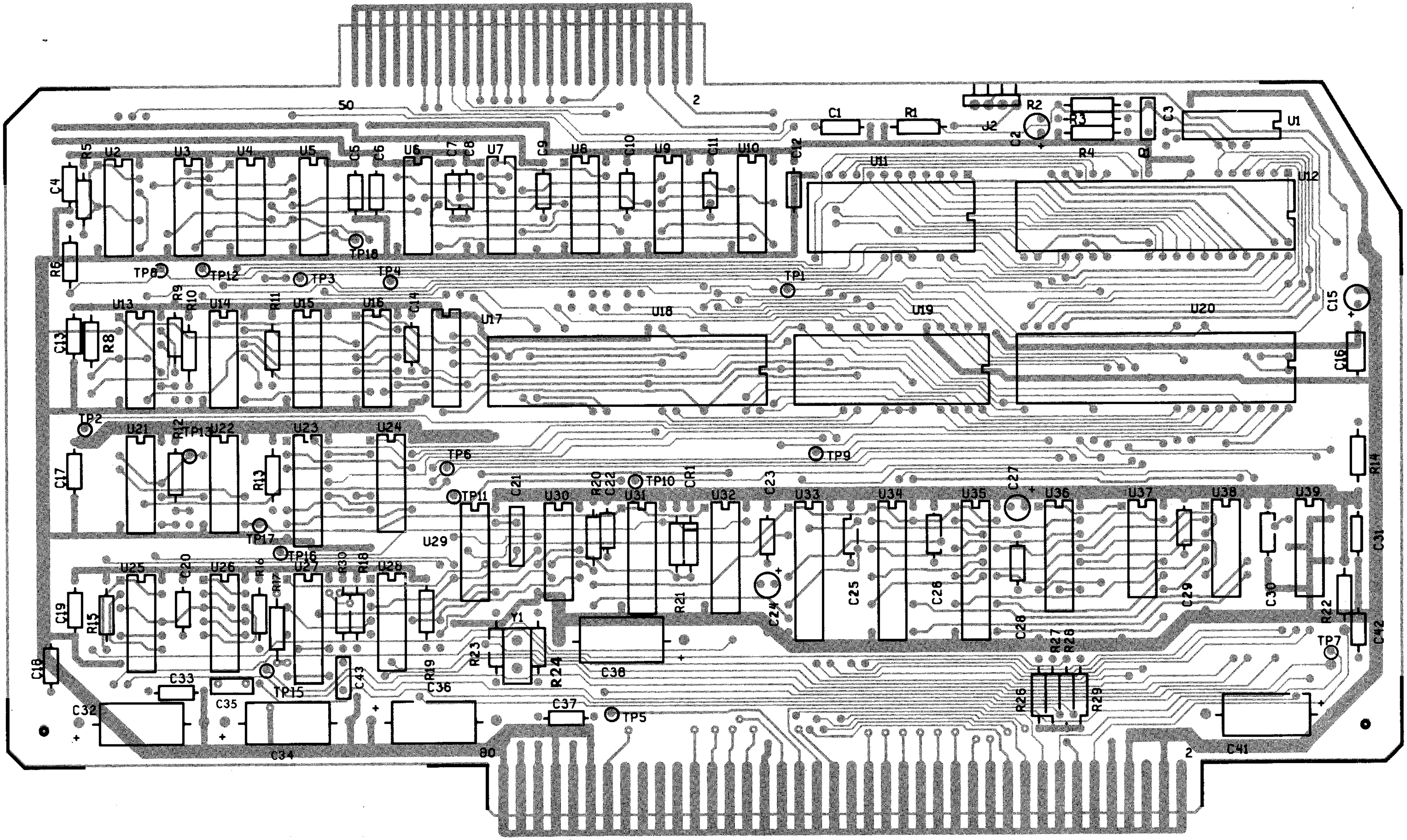


Figure 1. X-Ray View CPU Printed Circuit Board — Component Side

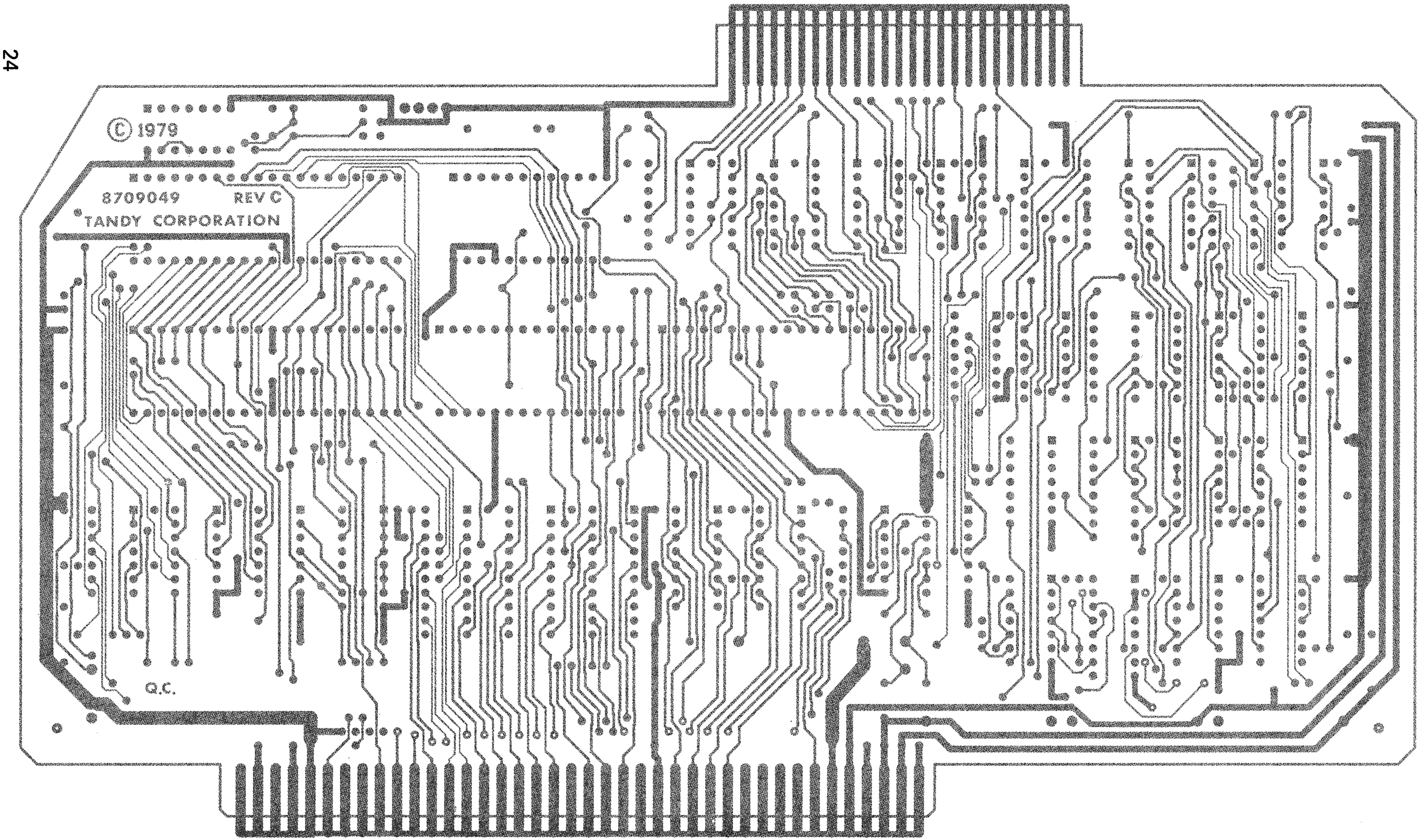


Figure 2. X-Ray View CPU Printed Circuit Board — Circuit Side

CPU MODULE PARTS LIST

SYMBOL	DESCRIPTION	MANUFACTURER'S PART NUMBER	RADIO SHACK PART NUMBER
	ELECTRICAL		
	PC Board	8709040	———
	CAPACITORS		
C1	0.1μF, 50V, Monolithic	8374104	———
C2	33μF, 50V, Electrolytic, Radial	8326331	ACC336QJAP
C3	33pF, 50V, Ceramic Disc	8300334	ACC330QJCP
C4	0.1μF, 50V, Monolithic	8374104	———
↓	↓ ↓	↓	↓
C14	0.1μF, 50V, Monolithic	8374104	———
C15	33μF, 50V, Electrolytic Radial	8326331	ACC336QJAP
C16	0.1μF, 50V, Monolithic	8374104	———
↓	↓ ↓	↓	↓
C20	0.1μF, 50V, Monolithic	8374104	———
C21	470pF, 50V, Ceramic Disc	8301474	ACC471QJCP
C22	0.1μF, 50V, Monolithic	8374104	———
C23	0.1μF, 50V, Monolithic	8374104	———
C24	33μF, 50V, Electrolytic, Radial	8326331	ACC336QJAP
C25	0.1μF, 50V, Monolithic	8374104	———
C26	0.1μF, 50V, Monolithic	8374104	———
C27	33μF, 50V, Electrolytic, Radial	8326331	ACC336QJAP
C28	0.1μF, 50V, Monolithic	8374104	———
↓	↓ ↓	↓	↓
C31	0.1μF, 50V, Monolithic	8374104	———
C32	33μF, 50V, Electrolytic, Axial	8316334	ACC336QJAA
C33	0.1μF, 50V, Monolithic	8374104	———
C34	33μF, 50V, Electrolytic, Axial	8316334	ACC336QJAA
C35	1000pF, 50V, Ceramic Disc	8303104	ACC102QJCP
C36	33μF, 50V, Electrolytic, Axial	8316334	ACC336QJAA
C37	0.1μF, 50V, Monolithic	8374104	———
C38	100μF, 16V, Electrolytic, Axial	8317101	ACC107QDAA
C39	Not Used	———	———
C40	Not Used	———	———
C41	33μF, 50V, Electrolytic, Axial	8316334	ACC366QJAA
C42	0.1μF, 50V, Monolithic	8374104	———
C43	33μF, 50V, Monlithic, Radial	8326331	ACC336QJAP
	INTEGRATED CIRCUITS		
U1	74S04, Hex inverter	8010004	———
U2	74LS74, Dual "D" flip-flop positive-edge-triggered	8020074	AMX3558
U3	74LS32, Quad 2-input OR gate	8020032	AMX3557
U4	74LS08, Quad 2-input AND gate	8020008	AMX3698
U5	74LS32, Quad 2-input OR gate	8020032	AMX3557
U6	MC1488, Quad line driver	8011488	———
U7	MC1488, Quad line driver	8011488	———
U8	MC1489, Quad line receiver	8011489	———

CPU MODULE PARTS LIST (Cont'd)

SYMBOL	DESCRIPTION	MANUFACTURER'S PART NUMBER	RADIO SHACK PART NUMBER
	INTEGRATED CIRCUITS (Cont'd)		
U9	MC1489, Quad line receiver	8011489	———
U10	MC1489, Quad line receiver	8011489	———
U11	2316E Mask ROM, 450ns access	8043316	———
U12	Z80A, CPU	8047880	AXX3014
U13	74LS74, Dual "D" flip-flop positive-edge-triggered	8020074	AMX3558
U14	74LS08, Quad 2-input AND gate	8020008	AMX3698
U15	74S00, Quad 2-input NAND gate	8010000	———
U16	74LS32, Quad 2-input AND gate	8020008	AMX3557
U17	74LS04, Hex inverter	8020004	AMX3552
U18	Z80A, SIO	8047884	AMX3018
U19	Z80A, CTC	8047882	AXX3016
U20	Z80A, DMA	8047883	AXX3017
U21	74LS32, Quad 2-input OR gate	8020032	AMX3557
U22	74LS10, Triple 3-input NAND gate	8020010	AMX3898
U23	74S182, Look-ahead carry generator	8010182	———
U24	74S04, Hex inverter	8010004	———
U25	74LS74, Dual "D" flip-flop positive-edge-triggered	8020074	AMX3558
U26	74LS74, Dual "D" flip-flop positive-edge-triggered	8020074	AMX3558
*U27	74LS121, Monostable multivbrator	8000121	———
U28	74LS74, Dual "D" flip-flop positive-edge-triggered	8020074	AMX3558
U29	74LS04, Hex inverter	8020004	AMX3552
U30	74LS132, Quad 2-input positive NAND Schmitt Trigger	8020132	AMX3561
U31	8T26A, Bus transceiver	8060026	AMX4261
U32	8T26A, Bus transceiver	8060026	AMX4261
U33	74LS244, Line driver	8020244	AMX3864
U34	74LS240, Line driver	8020240	AMX4225
U35	74LS240, Line driver	8020240	AMX4225
U36	74LS145, BCD-to-Decimal decoder	8020145	———
U37	74LS20, Dual 4-input NAND gate	8020020	AMX3555
U38	74LS32, Quad 2-input OR gate	8020032	AMX3557
U39	74LS125, Quad bus buffer gate with three state outputs	8020125	———
*On C revision boards and above, U27 will appear as:			
U27	74LS123, Monostable multivibrator	8020123	AMX3803
	CRYSTAL		
Y1	8.00MHz, 18pF, loading capacity	8409006	AMX2571
	DIODE		
CR1	1N4148, Silicon	8150148	ADX1152

CPU MODULE PARTS LIST (Cont'd)

SYMBOL	DESCRIPTION	MANUFACTURER'S PART NUMBER	RADIO SHACK PART NUMBER
	JACK		
J2	Connector, 4-position header	8519053	AJ6791
	TRANSISTOR		
Q1	2N3906, PNP	8100906	AMX3584
	RESISTORS		
R1	330 ohm, 1/4W, 5%, Carbon Film	8207133	AN0159EEC
R2	1.2K, 1/4W, 5%, Carbon Film	8207212	AN0199EEC
R3	220 ohm, 1/4W, 5%, Carbon Film	8207122	AN0149ECC
R4	22 ohm, 1/4W, 5%, Carbon Film	8207022	AN0078EEC
R5	2.2K, 1/4W, 5%, Carbon Film	8207222	AN0216EEC
R6	4.7K, 1/4W, 5%, Carbon Film	8207247	AN0247EEC
R7	Not Used	———	———
R9	4.7K, 1/4W, 5%, Carbon Film	8207247	AN0247EEC
R10	2.2K, 1/4W, 5%, Carbon Film	8207222	AN0216EEC
R11	2.2K, 1/4W, 5%, Carbon Film	8207222	AN0216EEC
R12	2.2K, 1/4W, 5%, Carbon Film	8207222	AN0216EEC
R13	2.2K, 1/4W, 5%, Carbon Film	8207222	AN0216EEC
R14	10K, 1/4W, 5%, Carbon Film	8207310	AN0281EEC
R15	2.2K, 1/4W, 5%, Carbon Film	8207222	AN0216EEC
R16	2.2K, 1/4W, 5%, Carbon Film	8207222	AN0216EEC
R17	47K, 1/4W, 5%, Carbon Film	8207347	AN0340EEC
R18	2.2K, 1/4W, 5%, Carbon Film	8207222	AN0216EEC
R19	2.2K, 1/4W, 5%, Carbon Film	8207222	AN0216EEC
R20	2.2K, 1/4W, 5%, Carbon Film	8207222	AN0216EEC
R21	10K, 1/4W, 5%, Carbon Film	8207310	AN0281EEC
R22	2.2K, 1/4W, 5%, Carbon Film	8207222	AN0216EEC
R23	910 ohm, 1/4W, 5%, Carbon Film	8207191	AN0192EEC
R24	910 ohm, 1/4W, 5%, Carbon Film	8207191	AN0192EEC
R25	Not Used	———	———
R26	2.2K, 1/4W, 5%, Carbon Film	8207222	AN0216EEC
R27	2.2K, 1/4W, 5%, Carbon Film	8207222	AN0216EEC
R28	2.2K, 1/4W, 5%, Carbon Film	8207222	AN0216EEC
R29	2.2K, 1/4W, 5%, Carbon Film	8207222	AN0216EEC
R30	10K, 1/4W, 5%, Carbon Film	8207310	AN0281EEC
	MISCELLANEOUS		
	Plug, Jumper (7)	8519021	AJ6769
	Reset Switch Assembly	8893001	AW2433
	Socket, IC, 24-pin	8509001	AJ6579
	Socket, IC, 28-pin	8509007	AJ6758
	Socket, IC, 40-pin (3)	8509002	AJ6580
	Spacer, Crystal	8589004	AHB9424
	Staked Pins (31)	8529014	AHB9682

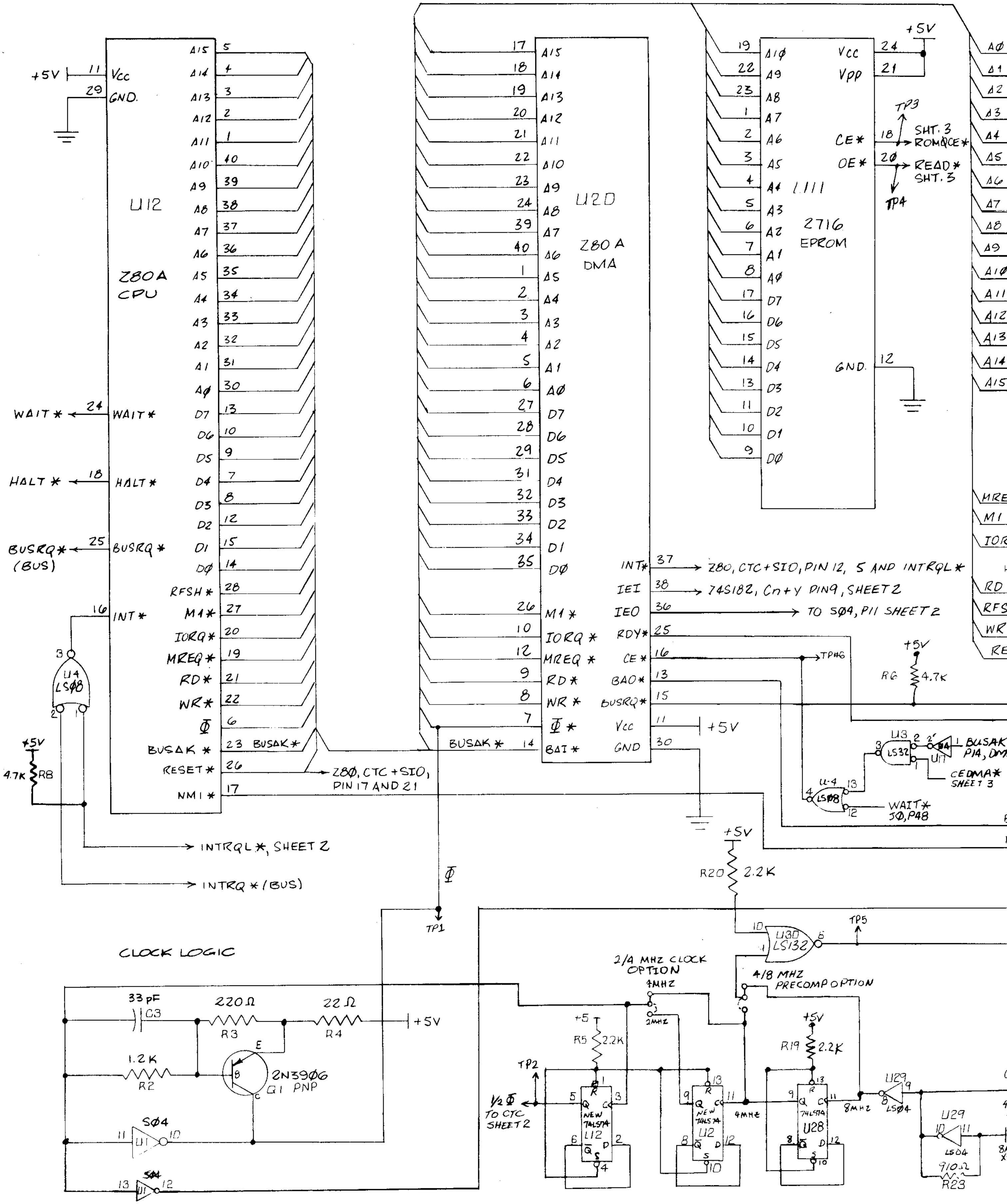
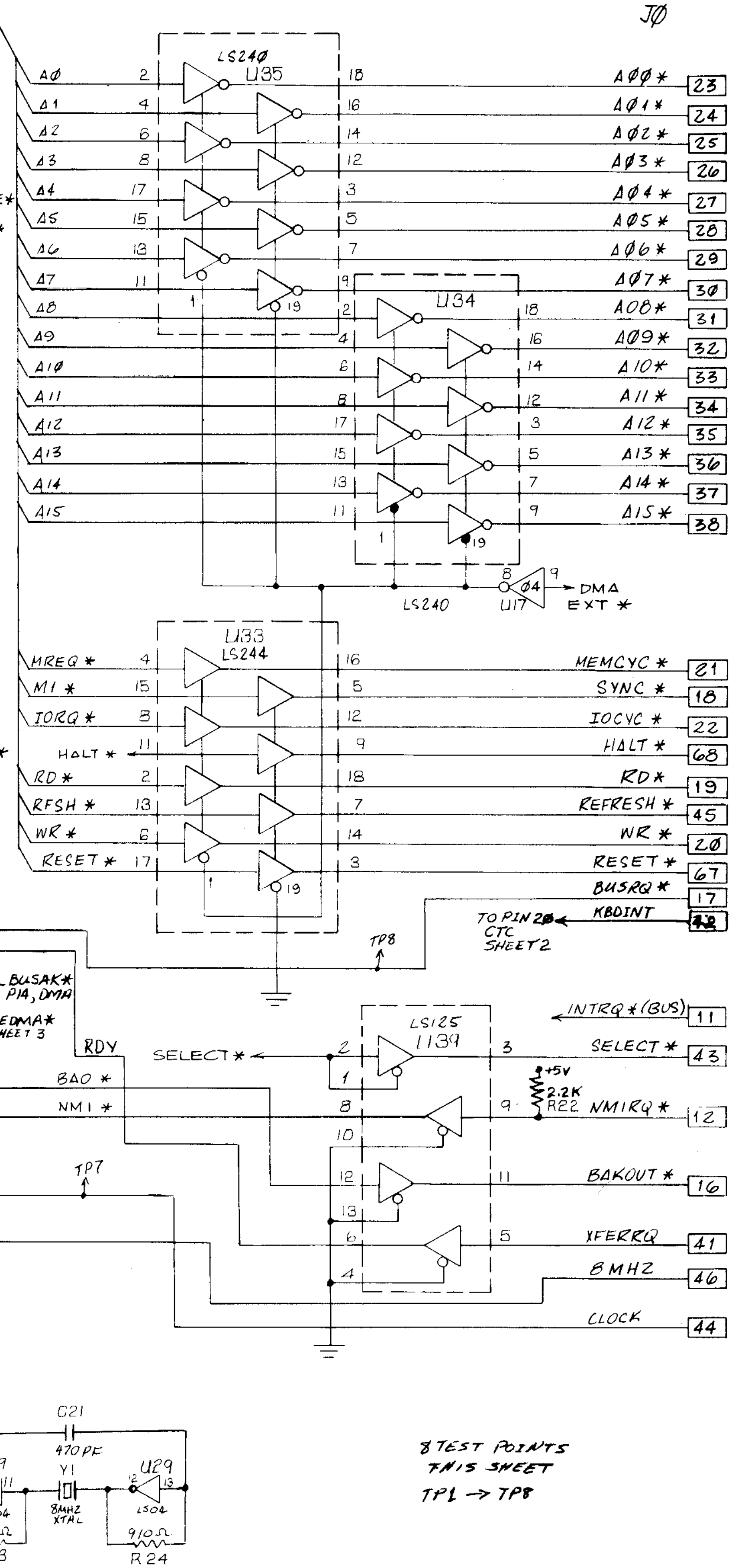


Figure 3. CPU Schemat



chematic Diagram — Sheet 1

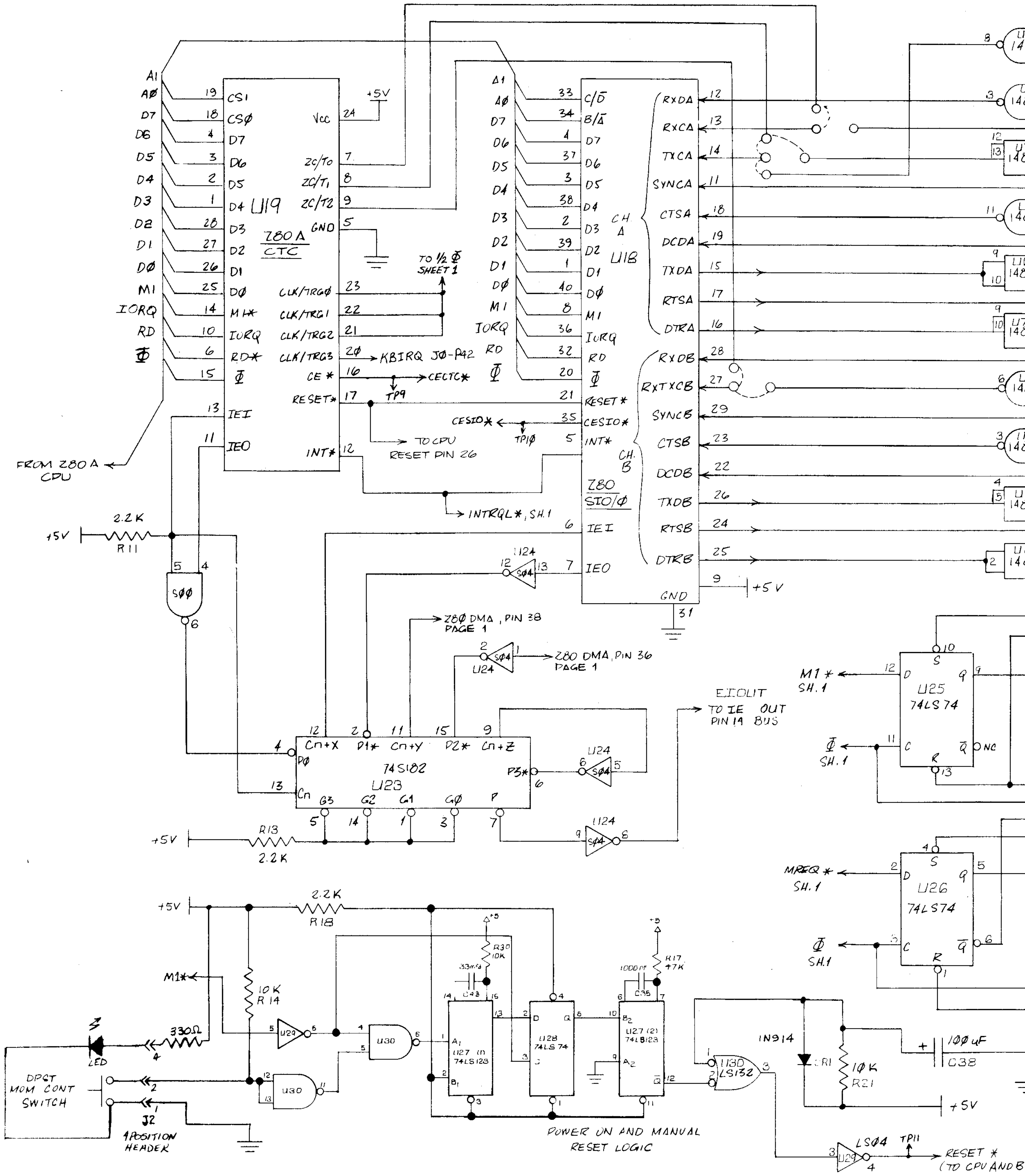
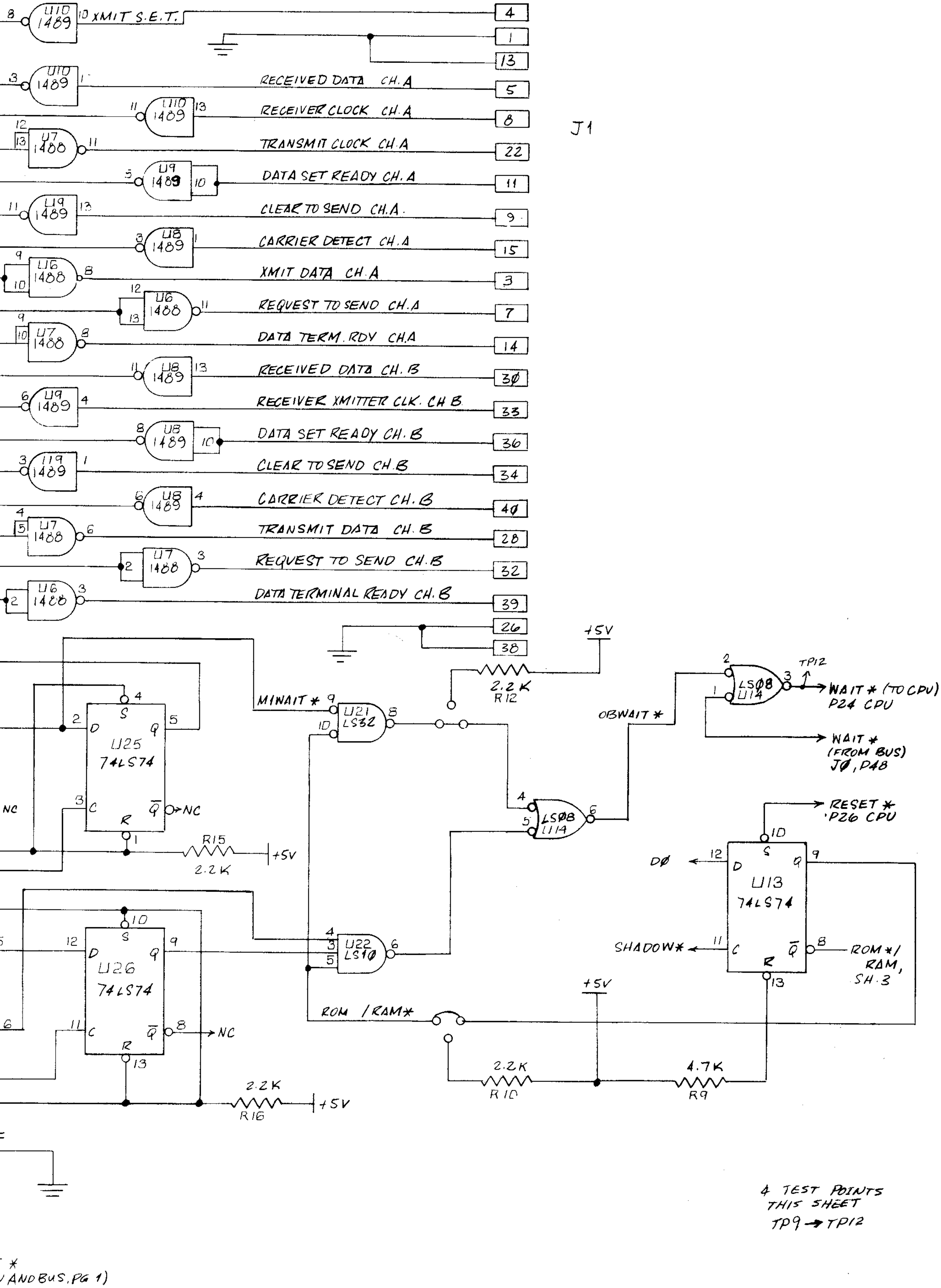


Figure 3. CPU Schematic Dia



tic Diagram — Sheet 2

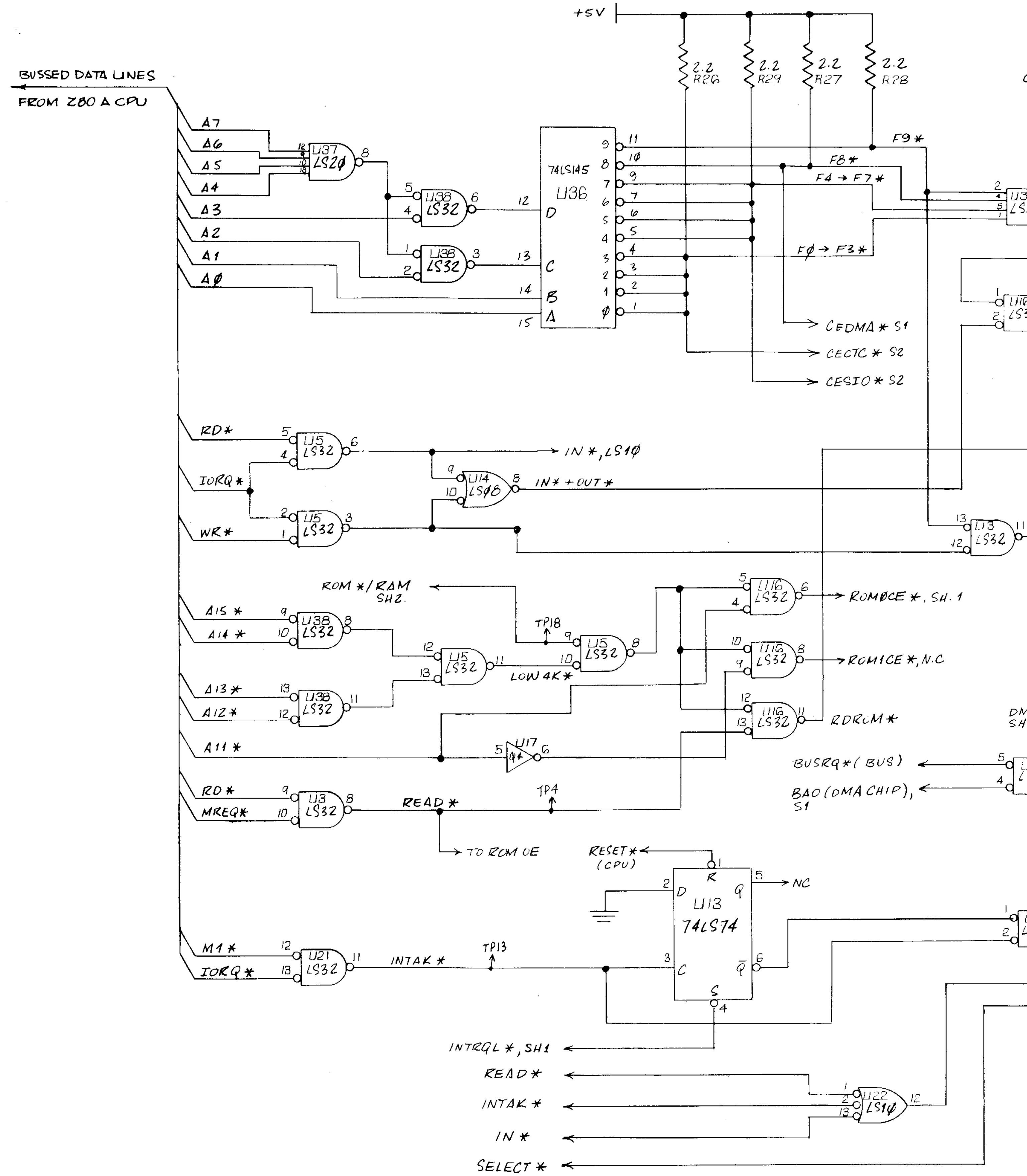
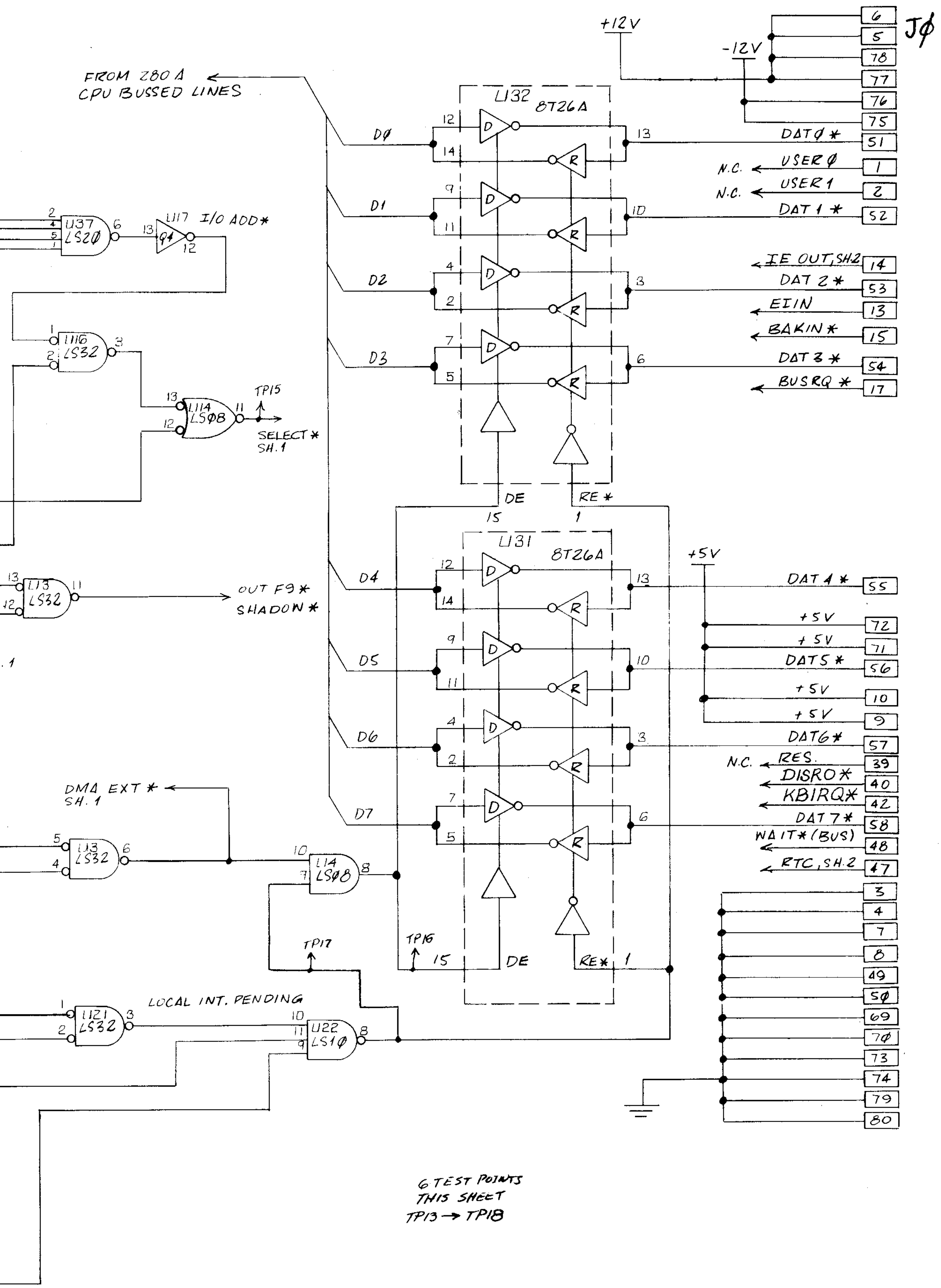


Figure 3. CPU Schema



PU Schematic Diagram — Sheet 3

SECTION IV

FLOPPY DISK CONTROLLER

A. FUNCTIONAL SPECIFICATIONS

The TRS-80 MODEL II FDC – PRINTER INTERFACE BOARD provides a standard 8" floppy disk interface and a Centronics parallel printer interface. The floppy disk interface supports both single and double density encoding schemes. Jumper options are also provided to select various write precompensation schemes. The data-clock recovery logic incorporates a phase locked loop oscillator which achieves state-of-the-art reliability. A write current switch signal is provided at the drive interface for drivers which require this feature. One to four drives may be controlled by the interface. The programmer has the option of using either CPU Data transfers or Direct Memory Access transfers if operating in the single density mode. However, if operating in the double density mode, all data transfers must be by Direct Memory Access. Status checking may be accomplished in polled or interrupt modes but not both at the same time. Interrupts may be generated for various conditions present on the drive status lines (ie. two sided diskette in drive, drive door opened since last select, drive not ready, etc.) Head load settling time is managed completely by the hardware and is therefore transparent to the programmer.

The printer interface is fully compatible with the various Radio Shack line printers as well as other printers which conform to the Centronics parallel standard. Interrupts may be generated on a character by character basis or only after the completion of a time consuming operation such as carriage returns, line feeds, or form feeds.

B. THEORY OF OPERATION

Decoding Logic

The FDC-PRINTER INTERFACE BOARD is an I/O port mapped device which utilizes ports EØH through E7H and port EFH. Port mapped devices use the lower eight address bits only to specify which port is being addressed. The upper eight address bits are ignored completely and are not relevant to port mapped devices. Three other signals (WR*, RD* and IOCYC*) are used by port mapped devices to determine whether an input or an output operation is to occur. If RD* and IOCYC* are both low, this condition specifies that an input from the addressed port is in progress. If WR* and IOCYC* are both low, this condition specifies that an output to the addressed port is in progress.

Page one of the FDC schematic should now be referred to for the remainder of the Decoding Logic discussion. U20, pin 6 is the output of a four input NAND gate. This pin should be low when any of the ports EØH through EFH are being addressed. U20, pin 8 is also an output of a four input NAND gate which should go low when the port being addressed contains an F HEX in the low order nibble of the port address.

These two outputs are combined at pins 13 and 12 of U8 to produce a low going strobe at pin 11 of U8. SELECTI* should go low any time an input or output operation to the used ports occurs. This signal is buffered with an open collector driver (U34) and connected to pin 43 of the system bus. Pin 43 (SELECT*) can be monitored with a scope while executing a diagnostic program to verify proper operation of the decoding logic.

CPUIN is a signal generated by the decoding logic for the purpose of switching the direction of the data bus transceivers (U32, U33) in preparation for an input operation. There are two conditions which require the data bus transceivers to switch direction such that they drive data outward to the system data bus. One is a port input operation and the other is an interrupt acknowledge cycle.

The first condition is detected by the combination of any of the ports EØH through E7H being addressed, concurrent with an input operation in progress. U19, pin 6 should go low when this condition is detected. If SYNCI* and IOCYCI* are both low, this condition indicates that an interrupt acknowledge cycle is in progress and that the interrupting device should present its vector to the data bus.

IOCYCI* and WRI* are combined at pins 1 and 2 of U21 to produce an active low signal (OUT*) at pin 3 of U21. This pin should be low any time an output instruction is being executed.

OUT* is combined with the output from pin 11 of U8 and pins 4 and 5 of U21 to produce the output DRVSLT* at pin 6 of U21. The rising edge of DRVSLT* is used by pin 9 of U17 to latch the data present on the internal data bus corresponding to an output to port EFH.

This data pattern is used to determine the drive, mode, and side selection. The bit allocation for this latch is detailed in the Port Allocation section of this manual.

The output of pin 6 of U20, designated EX*, is combined with A31 at pins 1 and 2 of U8 to produce a low at pin 3 of U8, which corresponds to port addresses EØ through E7. The output of pin 3 of U8 is combined with A21 at pins 9 and 10 of U8, to produce a low at pin 8 of U8 corresponding to port addresses E3H through E7H. The output of U8 pin 8, labeled CEPIO*, is the chip enable signal for the Z8Ø PIO. The output of U8 pin 6, labeled CEFDC*, is the chip enable signal for the FD1791.

The output of U21 pin 8 is a signal labeled SELECTI* which is useful for diagnostic purposes.

Interrupt priority is determined by the signal IEIN (pin 13 of the system bus). During an interrupt acknowledge cycle if IEIN is high, this indicates that no device of higher priority is requesting service and that the requesting device may bring its IEOUT (pin 14 of the system bus) low to pre-

vent devices of lower priority from receiving service. A high on pin 1 of U13 indicates that an interrupt acknowledge cycle is in progress. A high on pin 2 of U13 indicates that no higher priority device is requesting service. A high on pin 13, U13 indicates that a device on this board is requesting service. If all of these conditions are true, pin 12 of U13 should go low. This output is combined with the output from pin 6 of U19 and pins 4 and 5 of U10. If either pin 4 or pin 5 of U10 goes low, then pin 6 of U10 will also go low. U18 inverts the signal from pin 6 of U10 and causes pin 8 of U18 to go high (CPUIN). A high on CPUIN forces the data bus transceivers (U32, U33) to disable its receivers and enable its drivers to gate data onto the system bus. This allows the PIO to transfer its interrupt vector to the CPU.

Bus Interface Logic

Good design practice dictates that most signals to and from the system bus must be buffered so that only one TTL Load is presented to each signal line. Page one of the FDC schematic shows the logic required to implement this. U35 is an octal inverting buffer for the address lines. U36 is an octal non-inverting buffer for the Z8Ø control lines. Note that the enables for both these parts are tied low, allowing these signals to be gated onto the board at all times. U34 is an open collector buffer used to drive the board outputs which may be driven by other boards in the system. It also buffers the system clock (2 or 4MHz) to the board. U14 is ½ of a "D" Flip-Flop configured as a divide by two counter. This divider should be jumpered A to B if the system clock is 4MHz (normal connection), or B to C if a 2MHz system clock is used.

There is a basic problem with using a Z80-PIO with the FD1791. The PIO has a non-inverting data bus while the FD1791 utilizes an inverting data bus. Thus, one extra stage of inversion is required for the PIO. U23, U11, and U12 accomplish this extra inversion.

Z8Ø – PIO Interface Logic

The Z8Ø parallel I/O (PIO) interface controller is a general purpose, programmable, two port device which provides TTL compatible interfacing between peripheral devices and the Z8Ø –CPU. Any of the following modes can be selected for either port.

BYTE OUTPUT
BYTE INPUT
BYTE BIDIRECTIONAL (PORT A ONLY)
BYTE OR CONTROL MODE

In addition the PIO provides a clean and minimal logic method for generating mode 2 interrupts to the Z80 CPU.

Port A is used in the control mode which allows the eight I/O lines (AØ through A7) to be configured as either inputs or outputs. An 8-bit mask register and a 2-bit mask control register allow interrupts to be generated dependent upon the logic states of the I/O lines. Port A is primarily used for status checking and generating interrupts. One I/O line is configured as an output and provides the prime signal for the printer interface. The bit allocations for this port are detailed in the Port Allocations section of this manual.

Port B is used in the output mode for the purpose of outputting characters to the printer. The outputs of port B (BØ through B7) are isolated from the printer with an octal noninverting buffer (U24). Note that the enables are tied low, gating whatever data is presented to the inputs of U24 directly to its outputs. The cable to the printer allows this parallel data to be routed to the printer. Pin 21 of the PIO, labeled BRDY, produces a high going pulse which indicates that valid data is present on the port B outputs. The rising edge of this signal provides a trigger for pin 3 of U37. U37 is a one-shot which produces a 1.5μs low going pulse when triggered. The rising edge of the 1.5μs strobe is used by the printer to latch the 8 bits of information present on the output of U24. The BRDY signal stays active until the rising edge of PACK* which indicates that the printer has accepted the data. This rising edge may also generate an interrupt if the interrupt enable Flip-Flop is set and the PIO has the highest priority. This provides a clean and efficient method for determining when the printer can accept a new character without using status checking loops.

The PIO interfaces directly to the system bus with a minimum of external components. DØ through D7 form a bidirectional data path to the system bus. AØI and A1I determine which port is addressed and whether the operation is intended for the command register or the data register. If CEPIO*, IORQI* and RDI* are all low, this indicates an input operation is in progress. If CEPIO* and IORQI* are low with RDI* high, this indicates an output operation is in progress. If IEIN is high, and INTRQI*, SYNCI*, IORQI* and IEO are low, an interrupt acknowledge cycle for the PIO is in progress. If SYNCI* is high and RESETI* is low, a low is generated on pin 3 of U10. If this sequence occurs without RDI* or IORQI* low, the PIO logic enters a reset state. For a more detailed discussion of the PIO operation, consult the ZILOG Z8Ø – PIO Technical Manual.

FD1791 – Floppy Disk Controller IC

The FD1791 is an MOS LSI device which performs the functions of a Floppy Disk format/controller in a single chip implementation. The FD1791 contains all the features of its predecessor, the FD1771, plus the added features necessary to read, write, and format a double density diskette. These include address mask detection, FM and MFM encode and decode logic, window extension, and write precompensation.

FD1791 Organization

The Floppy Disk Formatter block diagram is illustrated in Figure 1. The primary sections include the parallel Processor Interface and the Floppy Disk Interface.

Data Shift Register — This 8-bit register assembles serial data from the Read Data input (RAW READ) during Read operations and transfers serial data to the Write Data output during Write operations.

Data Register — This 8-bit register is used as a holding register during Disk Read and Write operations. In Disk Read operations, the assembled data byte is transferred in parallel to the Data Register from the Data Shift Register. In Disk Write operations, information is transferred in parallel from the Data Register to the Data Shift Register. When executing the Seek command the Data Register holds the address of the desired Track position. This register can be loaded from the $\overline{DAL}$ and gated onto the $\overline{DAL}$ under processor control.

Track Register — This 8-bit register holds the track number of the current Read/Write head position. It is incremented by one every time the head is stepped in (towards track 76) and decremented by one when the head is stepped out (towards track Ø). The contents of the register are compared with the recorded track number in the ID field during disk Read, Write, and Verify operations. The Track Register can be loaded from or transferred to the $\overline{DAL}$. This Register should not be loaded when the FDC is busy.

Sector Register (SR) — This 8-bit register holds the address of the desired sector position. The contents of the register are compared with the recorded sector number in the ID field during disk Read or Write operations. The Sector Register contents can be loaded from or transferred to the $\overline{DAL}$. This register should not be loaded when the FDC is busy.

Command Register (CR) — This 8-bit register holds the command presently being executed. This register should not be loaded when the FDC is busy unless the execution of the current command is to be overridden. This latter action results in an interrupt. The command register can be loaded from the $\overline{DAL}$, but not read onto the $\overline{DAL}$.

Status Register (STR) — This 8-bit register holds device Status information. The meaning of the Status bits is a function of the contents of the Command Register. This register can be read onto the $\overline{DAL}$, but not loaded from the $\overline{DAL}$.

CRC Logic — This logic is used to check or to generate the 16-bit Cyclic Redundancy Check (CRC). The CRC includes all information starting with the address mark and up to the CRC characters. The CRC register is preset

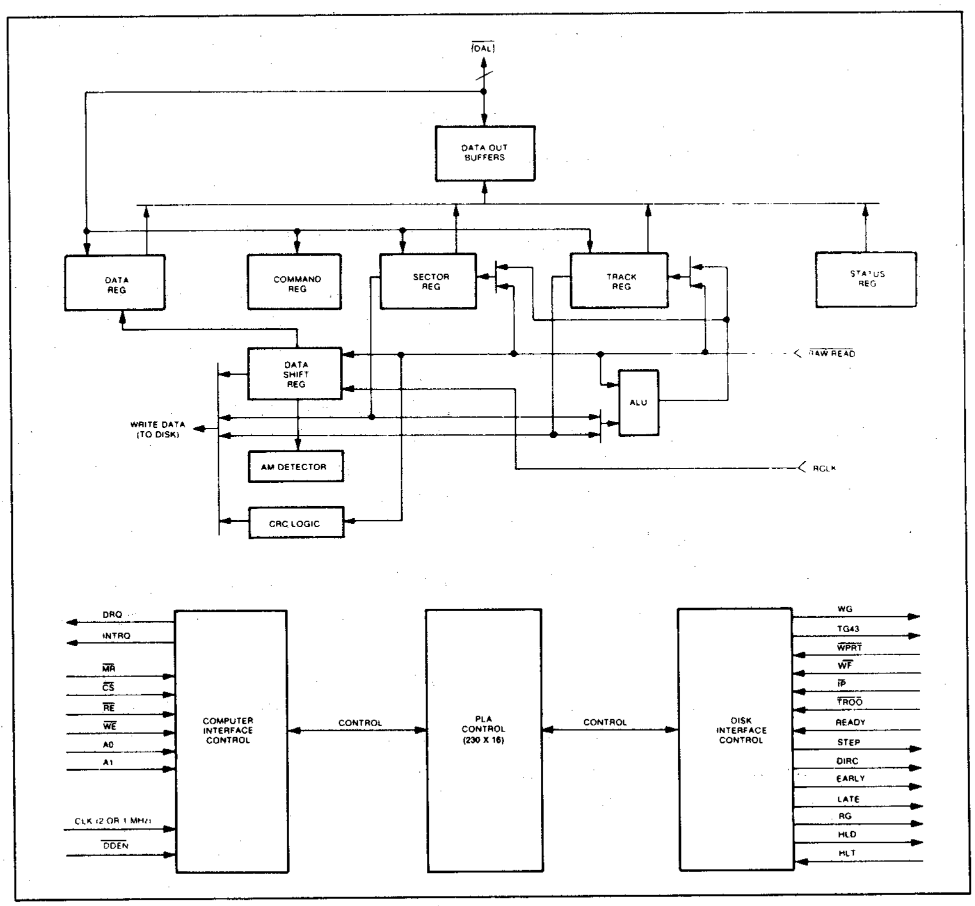


Figure 1. FD1791 Block Diagram

to ones (1's) prior to data being shifted through the circuit.

Arithmetic/Logic Unit (ALU) — The ALU is a serial comparator, incrementer, and decrementer and is used for register modification and comparisons with the disk recorded ID field.

Timing and Control — All computer and Floppy Disk Interface controls are generated through this logic. The internal device timing is generated from an external crystal clock.

The FD1791 has two different modes of operation according to the state of $\overline{DDEN}$. When $\overline{DDEN}$ = Ø, double density (MFM) is assumed. When $\overline{DDEN}$ = 1, single density (FM) is assumed.

AM Detector — The address mark detector detects ID, data and index address marks during read and write operations.

Processor Interface

The interface to the processor is accomplished through the eight Data Access Lines ($\overline{DAL}$) and associated control signals. The $\overline{DAL}$ are used to transfer Data, Status, and Control words out of, or into the FD1791. The $\overline{DAL}$ are three-state buffers that are enabled as output drivers when Chip Enable (CE*) and Read Enable (RE*) are active (low logic state) or act as input receivers when CE* and Write Enable (WE*) are active.

When transfer of data to the Floppy Disk Controller is required by the host processor, the device address is decoded and CE* is made low. The least-significant address bits A1 and AØ, combined with the signals RE* during a Read operation or WE* during a Write operation, are interpreted as selecting the following registers:

Table 1. Register Select

PORT ADDRESS	A1 – AØ	READ (RE*)	WRITE (WE*)
E4H	Ø Ø	Status Register	Command Register
E5H	Ø 1	Track Register	Track Register
E6H	1 Ø	Sector Register	Sector Register
E7H	1 1	Data Register	Data Register

During Direct Memory Access (DMA) types of data transfers between the Data Register of the FD1791 and the processor, the Data Request (DRQ) output is used in Data Transfer control. This signal also appears as status bit 1 during Read and Write operations.

On Disk Read operation, the Data Request is activated (set high) when an assembled serial input byte is transferred in parallel to the Data Register. This bit is cleared when the Data Register is read by the processor or DMA Controller. If the Data Register is read after one or more characters are lost (by having new data transferred into the register prior to processor readout) the Lost Data bit is set in the Status Register. The Read operation continues until the end of the sector is reached.

On Disk Write operation, the Data Request is activated when the Data Register transfers its contents to the Data Shift Register and requires a new data byte. It is reset when the Data Register is loaded with new data by the processor or DMA controller. If new data is not loaded at the time the next serial byte is required by the Floppy Disk, a byte of zeroes is written on the diskette and the Lost Data bit is set in the Status Register.

At the completion of every command an INTRQ is generated. INTRQ is reset by either reading the status register or by loading the command register with a new command. In addition, INTRQ is generated if a Force Interrupt command condition is met.

Floppy Disk Interface

The FD1791 has two modes of operation according to the state of $\overline{DDEN}$ (pin 37). When $\overline{DDEN}$ = 1, single density is selected. When $\overline{DDEN}$ = Ø, double density is selected. In either case, the CLK input (pin 24) is at 2 MHz. When the clock is at 2MHz, the stepping rates of 3, 6, 10, and 15ms are obtainable.

Head Positioning

Four commands cause positioning of the Read-Write head (see Comand Section). The period of each positioning step is specified by the r field in bits 1 and Ø of the command word. After the last directional step, an additional 15 milliseconds of head settling time takes place if the Verify flag is set in Type I commands. Note that this time doubles to 30ms for a 1MHz clock. If TEST = Ø, there is zero settling time. There is also a 15ms head settling time if the E flag is set in any Type II or III command.

The rates (shown in Table 2) can be applied to a Step-Direction Motor through the device interface.

Step — A 2μs (MFM) or 4μs (FM) pulse is provided as an output to the drive. For every step pulse issued, the drive moves one track location in a direction determined by the direction output.

Direction (DIRC) — The Direction signal is active high when stepping in and low when stepping out. The Direction signal is valid 12μs before the first stepping pulse is generated.

When a Seek, Step, or Restore command is executed an optional verification of Read/Write head position can be performed by setting bit 2 (V = 1) in the command word to a logic 1. The verification operation begins at the end of the 15 millisecond settling time after the head is loaded against the media. The track number from the first encountered ID Field is compared against the contents of the Track Register. If the track numbers compare and the ID Field Cyclic Redundancy Check (CRC) is correct, the verify operation is complete and an INTRQ is generated with no errors. The FD1791 must find an ID field with correct track number and correct CRC within 5 revolutions of the media; otherwise the seek error is set and an INTRQ is generated.

The following example explains the use of the Stepping Rates Table:

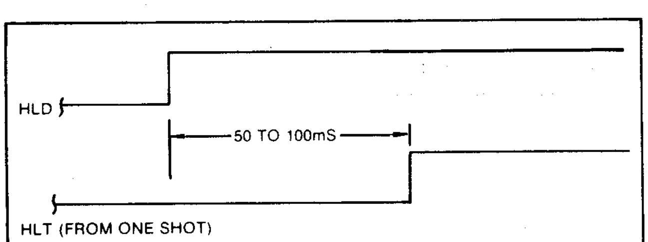
If Clock is 2MHz and DDEN (double density not) is high (1) and if bit R1 is low (Ø) while bit RØ is high (1) and TEST = 1, then the stepping time will be 6 milliseconds.

Table 2. Stepping Rates

CLK	2 MHz	2 MHz	1 MHz	1 MHz	2 MHz	1 MHz
DDEN	Ø	1	Ø	1	X	X
R1 RØ	TEST=1	TEST=1	TEST=1	TEST=1	TEST=Ø	TEST=Ø
Ø Ø	3 ms	3 ms	6 ms	6 ms	Approx.	Approx.
Ø 1	6 ms	6 ms	12 ms	12 ms	200μS	400μS
1 Ø	10 ms	10 ms	20 ms	20 ms		
1 1	15 ms	15 ms	30 ms	30 ms		

The Head Load (HLD) output controls the movement of the read/write head against the media. HLD is activated at the beginning of a Type I command if the h flag is set (h = 1), at the end of the Type I command if the verify flag is set (V = 1), or upon receipt of any Type II or III command. Once HLD is active it remains active until either a Type I command is received with (h = Ø and V = Ø); or if the FD1791 is in an idle state (non-busy) and 15 index pulses have occurred, it is reset.

Head Load Timing (HLT) is an input to the FD1791 which is used for the head engage time. When HLT = 1, the FD1791 assumes the head is completely engaged. The head engage time is typically 30 to 100 ms depending on drive. The low to high transition on HLD is used to fire a one shot (½ of U31). The output of the one shot is then used for HLT and supplied as an input to the FD1791.



Head Load Timing

When both HLD and HLT are true, the FD1791 will then read from or write to the media. The "and" of HLD and HLT appears as a status bit in Type I status.

In summary for the Type I commands: if h = Ø and V = Ø, HLD is reset. If h = 1 and V = Ø, HLD is set at the beginning of the command and HLT is not sampled nor is there an internal 15ms delay. If h = Ø and V = 1, HLD is set near the end of the command, an internal 15ms delay occurs, and the FD1791 waits for HLT to be true. If h = 1 and V = 1, HLD is set at the beginning of the command. Near the end of the command, after all the steps have been issued, an internal 15ms delay occurs and the FD1791 then waits for HLT to occur.

For Type II and III commands with E flag off, HLD is made active and HLT is sampled until true. With E flag on, HLD is made active, an internal 15ms delay occurs and then HLT is sampled until true.

Disk Read Operations

Sector lengths of 128, 256, 512, or 1024 are obtainable in either FM or MFM formats. For FM, DDEN should be placed to logical 1. For MFM formats, DDEN should be placed to a logical Ø. Sector lengths are determined at format time by a special byte in the ID field. If this Sector Length byte in the ID field is zero, then the sector length is 128 bytes. If Ø1, then 256 bytes. If Ø2, then 512 bytes. If Ø3, then the sector length is 1024 bytes. The number of sectors per track as far as the FD1791 is concerned can be from 1 to 255 sectors. The number of tracks as far as the FD1791 is concerned is from Ø to 255 tracks. For IBM 3740 compatibility, sector lengths are 128 bytes with 26 sectors per track. For System 34 compatibility (MFM), sector lengths are 256 bytes/sector with 26 sectors/track; or lengths of 1024 bytes/sector with 8 sectors/track.

For read operation, the FD1791 requires a RAW READ Data (Pin 27) signal which is a 250ns pulse per flux transition and a Read clock (RCLK) signal to indicate flux transition spacings. The RCLK (Pin 26) signal is provided by a Phase locked loop or counter techniques. In addition, a Read Gate Signal is provided as an output (Pin 25) which informs some phase locked loops when to acquire synchronization. When reading from the media in FM, RG is made true when 2 bytes of zeroes are detected. The FD1791 must find an address mark within the next 10 bytes; otherwise RG is reset and the search for 2 bytes of zeroes begins all over again. If an address mark is found within 10 bytes, RG remains true as long as the FD1791 is deriving any useful information from the data stream. Similarly for MFM, RG is made active true when 4 bytes of "ØØ" or "FF" are detected. The FD1791 must find an address mark within the next 16 bytes, otherwise RG is reset and search resumes.

Disk Write Operations

When writing is to take place on the diskette, the Write Gate (WG) output is activated. This allows current to flow into the Read/Write head. As a precaution to erroneous writing the first data byte must be loaded into the Data Register in response to a Data Request from the FD1791 before the Write Gate signal can be activated.

Writing is inhibited when the $\overline{\text{Write Protect}}$ input is a logic low, in which case any Write command is immediately terminated, an interrupt is generated, and the $\overline{\text{Write Protect}}$ status bit is set. The Write Fault input, when activated, signifies a writing fault condition detected in disk drive electronics such as failure to detect Write current flow when the Write Gate is activated. On detection of this fault the FD1791 terminates the current command, and sets the Write Fault bit (bit 5) in the Status Word. The Write Fault input should be made inactive when the Write Gate output becomes inactive.

For Write operation, the FD1791 provides Write Gate (pin 30) and Write Data (pin 31) outputs. Write Data consists of a series of 500ns pulses in FM ($\overline{\text{DDEN}}$ = 1) and 250ns pulses in MFM ($\overline{\text{DDEN}}$ = Ø). Write Data provides the unique address marks in both formats.

Also during write, two additional signals are provided for write precompensation. These are EARLY (Pin 17) and LATE (Pin 18). EARLY is active true when the WD pulse appearing on (Pin 30) is to be written early. EARLY is valid for the duration of the pulse. LATE is active true when the WD pulse is to be written late. If both are low when a WD pulse is present, the WD pulse is to be written at nominal.

Since write precompensation values vary from disk manufacturer to disk manufacturer, the actual value is determined by several one shots or delay lines which are located external to the FD1791. The write precompensation signals EARLY and LATE are valid in both FM and MFM formats.

Whenever a Read or Write command (Type II or III) is received the FD1791 samples the Ready input. If this input is logic low the command is not executed and an interrupt is generated. This also applies to Type I commands.

FDC and FDD Interface Logic

Drive, side, and mode selection must be accomplished external to the FD1791. A six-bit latched output port (U21) provides the outputs which control these functions. Note that the outputs from the FD1791 to the floppy drive interface are buffered with high current open collector inverting drivers (U4, U5, U16). This is required because the outputs of the FD1791 will directly drive only one standard TTL load.

Recording Codes

Information is stored on a disk using a code that takes the desired information and converts it to pulses that the recording system can write and recover from the disk. The ideal system requires that all the pulses written on the disk be information. The problem with this type of system is when the data is recovered it is not self-clocking. Self-clocking codes include Frequency Modulation (FM) and Modified Frequency Modulation (MFM). The actual flux reversal rate of the two codes is the same; the Table below shows the differences.

Table 3. Self-Clocking Codes

	DOUBLE FREQUENCY	MODIFIED FREQUENCY MODULATION
Bit Density	1836 3268	3672 (outer track) 6536 (inner track)
Data Transfer Rate	249,984 Hz	499,968 Hz
Bits/Track	42,664	83,328
Bits/Disk	3,208,128	6,416,256
Cell Time	4μs	2μs
Flux Density (inner track)	6536	6536

Frequency Modulation (FM): Information is always recorded by inserting a clock between each data bit. A "1" bit is defined as a flux transition between clocks while a Ø is defined as the absence of this flux transition. Clocks are always flux transitions.

Modified Frequency Modulation (MFM): Information is encoded using data and clocks such that the longest time between flux transitions is the same as in FM code but clocks are not recorded between data bits.

Definition:

1. "1" is defined as a flux transition occuring at the half cell time.
2. "Ø" is defined as a flux transition occuring at the start of the cell time. A pulse at the beginning of the cell is a clock; however, a clock is not always written. Clock is suppressed if there will be a "1" in this cell or if there was a "1" in the preceding cell.

Read Clock Recovery Logic

The read clock recovery logic is shown in Sheet 1 of the Floppy Disk Schematic (Figure 6). The block diagram below is included for reference.

A three input NAND gate (U13) insures that data and clock pulses are not allowed to enter the recovery circuit unless the FDD head is loaded and the settling time required has elapsed. The rising edge of these gated pulses triggers a one-shot (1/2 of U25).

The duty cycle of the output of this one-shot is determined by the adjustments performed on R36 and R37. R36 determines the timing for the FM mode, while R37 determines the timing for the MFM mode.

The other half of U25 is triggered by the falling edge of the pulses at pin 13 (U25), which produces a 150 ns pulse per flux transition at pin 12 of U25. This signal consists of both data and clock transitions and is fed directly to pin 27 of U6 (FD1791).

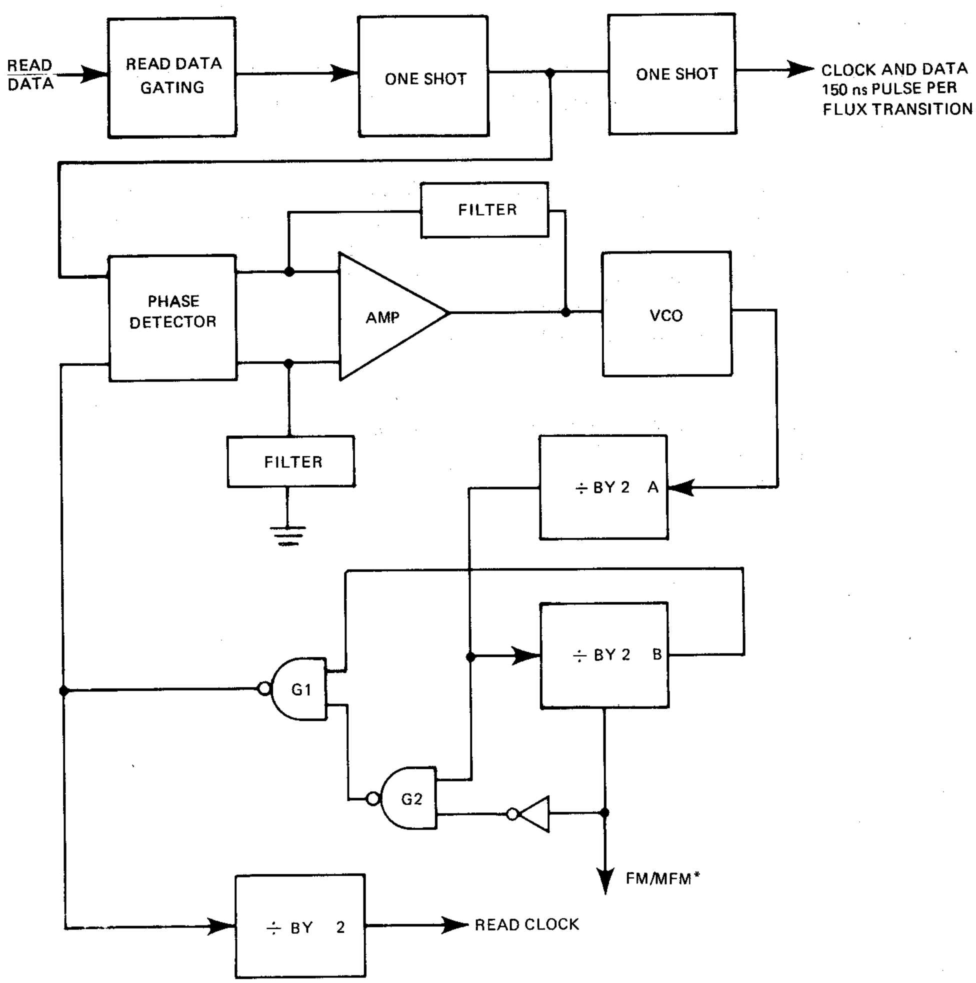


Figure 2. Clock Recovery Block Diagram

The phase locked loop oscillator circuit takes the pulses from pin 13 of U25 in either FM or MFM mode and develops a clock that is phase locked to the data. The main components of the circuitry include a phase detector, a filter/amplifier, a voltage controlled oscillator, and several stages of divide-by-two Flip-Flops. U28 is the phase detector which compares the phase of the pulse width shaped signal from pin 13 of U25 to the counted down VCO output. The output of pin 5 of U28 directs the VCO to increase the frequency while the output from pin 9 of U28 decreases the VCO frequency. U26, along with the associated feedback and filter components, combines, filters, and amplifies these two outputs, and produces a DC error voltage for the VCO. The VCO (U27) is an MC4024 of which only ½ is being used. The error signal from the amplifier is applied to pin 2 of U27 and the output (pin 6, U27) is applied to the divider circuit (U29) which is either a divide by 2 or a divide by 4, depending on whether MFM or FM mode is selected. The resulting signal is fedback to the phase detector to close the loop. This signal is presented to pin 3, U14 and is again divided by two and fed to a delay circuit implemented with two inverters (U4) and a NAND gate (U7). The output of pin 3, U7, is then fed to pin 26 of U6 which forms the read clock for the FDC.

Write Compensation

The write compensation circuit compensates for head/media peak shift. Peak shift is an effect that degrades read accuracy by distorting the waveform.

Ideally, the flux reversal command by the write toggle would be instantaneous. Current would immediately switch from one polarity to the other. However, it takes time for the current to reverse and the fields to decay and build up in the opposite direction. The resulting read back voltage is more or less sinusoidal with peaks less easily defined in time or amplitude.

With current recording techniques, adjacent clock/data pulses are close enough to interact with each other. This phenomenon is particularly noticeable at inner tracks. This is shown in Figure 3. Peak shift is the result of the interaction of the pulses. Because two pulses tend to have a portion of their individual signals superimposed on each other, the actual readback voltage is the algebraic summation of the pulses.

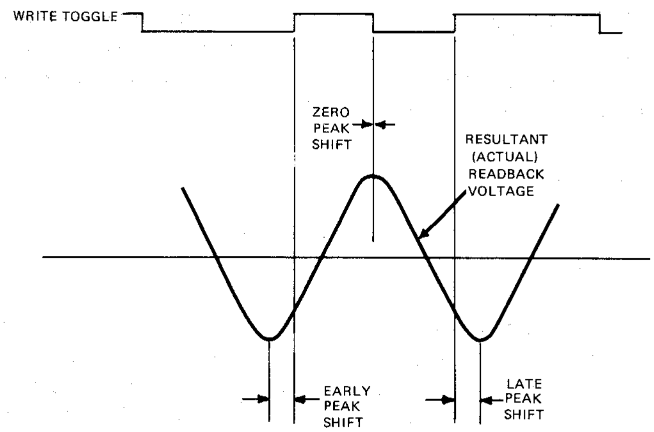


Figure 3. Interacting Clock/Data Pulses

When all 1's or all Ø's are being recorded, the data frequency is constant. Pulses are spaced apart by one cell. As a result, the pulse spacing causes the overlap errors to be equal and opposite. The negative-going and positive-going errors cancel each other. This is a "zero peak shift" condition.

Peak shift occurs when there is a change in frequency. A Ø11 pattern represents a frequency increase since there is a delay of about 1.5 cells between the Ø1 and only 1 cell between the 11. As a result, the squeezing of cells cause the mathematical average (the actual readback voltage) to shift the apparent peak to the left. This is early peak shift.

A 11Ø pattern represents a frequency decrease since a pulse is not written at all in the third cell.

Write compensation is required to reduce the effect of peak shift out of the head due to the reduced window of MFM data. The window is defined as the total amount of time that is allowed for the bit to appear and be recognized. The window of MFM is 1μs as opposed to the double frequency window of 2μs. The amount of compensation best suited to the present heads and media is 125 to 250ns. This compensation is applied to data patterns that will result in a large peak shift. The circuit looks at three bits on each side of a reference bit and determines whether to shift or not. The following patterns are compensated (bit shifted) in the direction of the arrow.

LATE	EARLY
→	←
XØ11	X11Ø
→	←
1ØØØ	ØØØ1

X = Don't Care

When a flux transition pattern of 11Ø is written on the disk the second 1 is pulled toward the Ø. Write compensation shifts this Ø in the opposite direction the amount of the expected shift.

Write Compensation Logic

Implementation

The write compensation logic is shown on page one of the FDC schematic. U1 forms a shift register which is clocked at 8MHz. This arrangement provides a predictable 125ns delay per stage for a logic one presented to pin 4 of U1.

The early, late, and TG43 signals from the FD1791, along with FM*/MFM, are gated through three AND gates (2/3 of U7) to control the operation of a Dual One of Four Data Selector (U2). The data selector gates one of its four inputs to the output, dependent upon the logic state of the A and B inputs. The top half of U2 is used for 125ns write precompensation while the lower half is used for 250ns precompensation.

The NAND gates (U3) to the right of U2 are used to select one of the two outputs from pins 7 or 9 of U2. Pin 7 of U2 is selected as the output if 125ns precompensation is used, while pin 9 of U2 is selected as the output if 250ns precompensation is used.

The output of U3 pin 1 is the compensated write data, which is used to trigger a one-shot (one-half of U37). A 250ns positive going pulse is produced at U37 pin 5 for every write pulse presented to U37 pin 10. The one-shot (U37) insures that the write data pulse width is always approximately 250ns. The output of the one-shot is buffered by a high current open collector driver (1/6 of U16) and presented to the floppy disk drive. When 250ns precompensation is used, it is necessary to stretch the late signal from the FD1791 approximately 500ns. Half of U31 (a one-shot) is used to produce the stretched late signal.

The table below describes the jumper options possible for the Write Compensation logic.

Table 4. Jumper Options

JUMPER CONNECTIONS	OPTION SELECTED
2 to 3 and 5 to 7	125ns outer TRKS 250ns inner TRKS
3 to 4 and 6 to 7	250ns inner only*
3 to 4 and 8 to 7	125ns inner only

*Standard System Configuration

As noted in the table, 250ns inner tracks only is the standard system configuration as shipped from the factory. Options other than the standard configuration should be used with caution and should not be attempted by the unexperienced user.

Table 5. Port Allocation

PORT #	ALLOCATION	FUNCTION
EØH	PIO Port A — Data	Printer and FDC INT. status
E1H	PIO Port B — Data	Printer Data (output)
E2H	PIO Port A — Control	Configuring Port A
E3H	PIO Port B — Control	Configuring Port B
E4H	FDC Status/CMD Register	FDC Status and CMD
E5H	FDC Track Register	Current Track Add.
E6H	FDC Sector Register	Current Sector Add.
E7H	FDC Data Register	Data To or From Diskette
EFH	Drive Select Latch	Drive, Mode, Side Select

Table 6. BIT Allocation
Port EFH, Drive Select Latch (output only)

D7	D6	D5	D4	D3	D2	D1	DØ
Mode Select	Side Select	Unused	Unused	DRV3SEL	DRV2SEL	DRV1SEL	DRVØSEL
1 = FM Mode	Ø = Side 1			1 = NOTSEL	1 = NOTSEL	1 = NOTSEL	1 = NOTSEL
1 = MFM Mode	1 = Side Ø			Ø = SEL	Ø = SEL	Ø = SEL	Ø = SEL

NOTE: D3 through DØ — only one of these bits should be low per output instruction.

Table 7. BIT Allocation
Port EØH, Printer, FDD, FDC Interrupt Status

D7	D6	D5
Printer Busy	Paper Empty	Printer Select
Ø = Not Busy	Ø = Paper not Empty	Ø = Selected
1 = Busy	1 = Paper Empty	1 = Not Selected
D4	**D3***	**D2***
Printer Fault	PRIME	Disk Change
Ø = Fault	High to Low	Ø = Door not Opened
1 = Not Fault	Transition Resets Printer	1 = Door Opened

D1	DØ
Two-Sided Diskette	FDC INT REQUEST
1 = Two-Sided Diskette Preset	1 = FDC is Interrupting
Ø = Single-Sided Diskette	Ø = Not Interrupting

*D2 indicates that the selected drive has had its door opened since it was last selected.

*D3 is an output which resets some printers.

J1 (FDC Board to Floppy Disk) SIGNAL DESCRIPTIONS

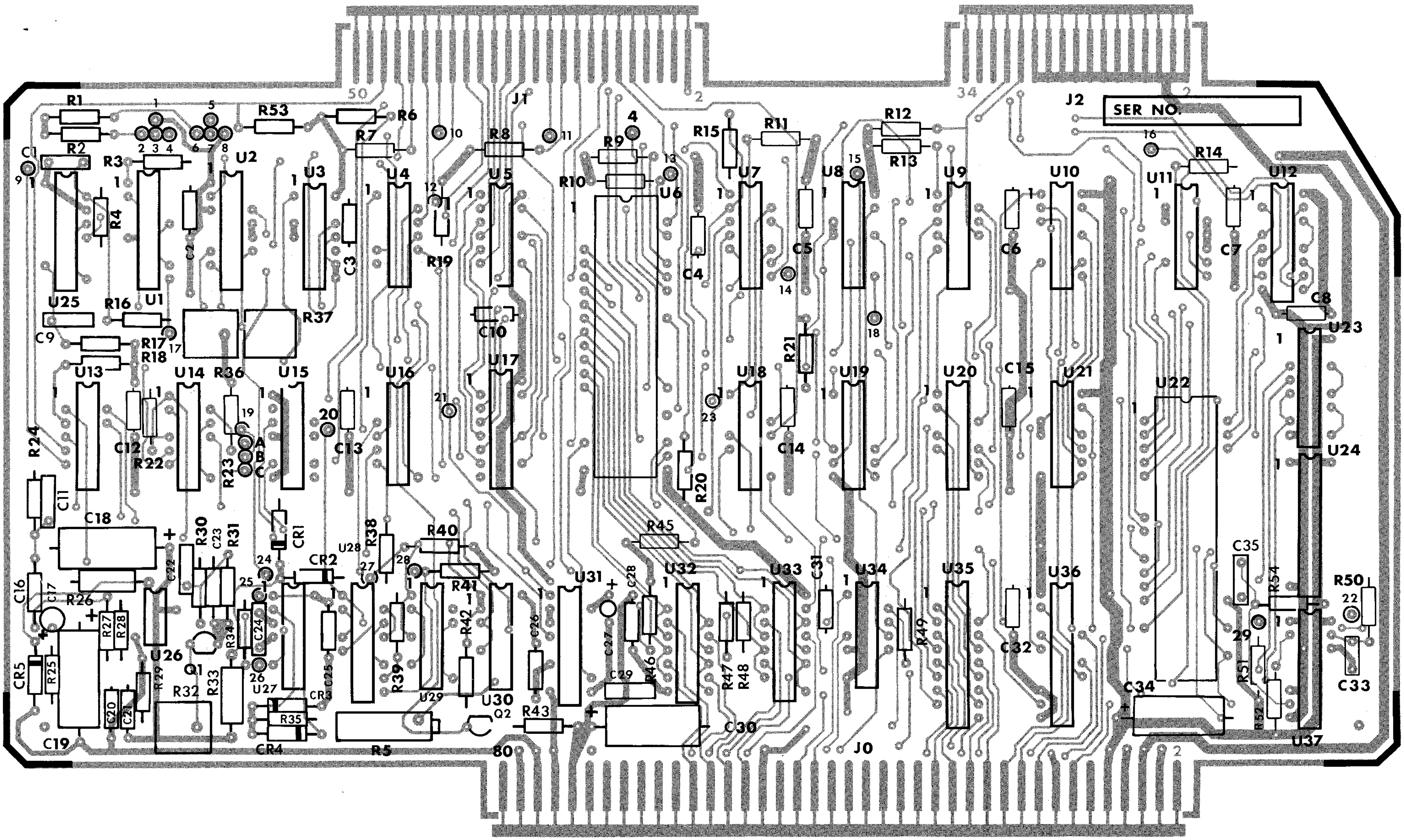
PIN	SIGNAL NAME	DESCRIPTION
1	GND	Power Ground
2	WRTCRT*	Reduced Write Current
3	GND	Power Ground
4	NC	Not Connected
5	GND	Power Ground
6	NC	Not Connected
7	GND	Power Ground
8	NC	Not Connected
9	GND	Power Ground
10	TWOSID*	Two Sided Diskette Installed
11	GND	Power Ground
12	DSKCHG*	Drive Door Opened Since Last Select
13	GND	Power Ground
14	SDSEL	Side Select; low = side Ø , high = side 1
15	GND	Power Ground
16	NC	Not Connected
17	GND	Power Ground
18	HLD*	Head Load
19	GND	Power Ground
20	IP*	Index Pusle
21	GND	Power Ground
22	RDY	Drive Ready
23	GND	Power Ground
24	NC	Not Connected
25	GND	Power Ground
26	DS1*	Drive Select One
27	GND	Power Ground
28	DS2*	Drive Select Two
29	GND	Power Ground
30	DS3*	Drive Select Three
31	GND	Power Ground
32	DS4*	Drive Select Four
33	GND	Power Ground
34	DIR*	Step Direction
35	GND	Power Ground
36	STEP*	Step Head One Track
37	GND	Power Ground
38	CPWD*	Write Data
39	GND	Power Ground
40	WG*	Write Gate
41	GND	Power Ground
42	TRKØ*	Track Zero Indication
43	GND	Power Ground
44	WPRT*	Write Protected Diskette
45	GND	Power Ground
46	RD*	Read Data
47	GND	Power Ground
48	NC	Not Connected
49	GND	Power Ground
50	NC	Not Connected

*Indicates an inverted signal or an active low signal.

J2 (FDC Board to Line Printer) SIGNAL DESCRIPTIONS

PIN	SIGNAL NAME	DESCRIPTION
1	PSTB*	Data Strobe
2	GND	Power Ground
3	PDAT Ø	Data Bit Ø to Printer
4	GND	Power Ground
5	PDAT 1	Data Bit 1 to Printer
6	GND	Power Ground
7	PDAT 2	Data Bit 2 to Printer
8	GND	Power Ground
9	PDAT 3	Data Bit 3 to Printer
10	GND	Power Ground
11	PDAT 4	Data Bit 4 to Printer
12	GND	Power Ground
13	PDAT 5	Data Bit 5 to Printer
14	GND	Power Ground
15	PDAT 6	Data Bit 6 to Printer
16	GND	Power Ground
17	PDAT 7	Data Bit 7 to Printer
18	GND	Power Ground
19	PACK*	Printer Data Acknowledge
20	GND	Power Ground
21	BUSY	Printer Busy
22	GND	Power Ground
23	PE	Paper Empty
24	GND	Power Ground
25	PSEL	Printer Selected
26	PRIME	Printer Reset
27	GND	Power Ground
28	FAULT	Printer Fault
29	NC	Not Connected
30	NC	Not Connected
31	GND	Power Ground
32	NC	Not Connected
33	GND	Power Ground
34	NC	Not Connected

*Indicates an inverted signal or an active low signal.



FDC PRINTER INTERFACE

Figure 4. X-Ray View FDC Printed Circuit Board — Component Side

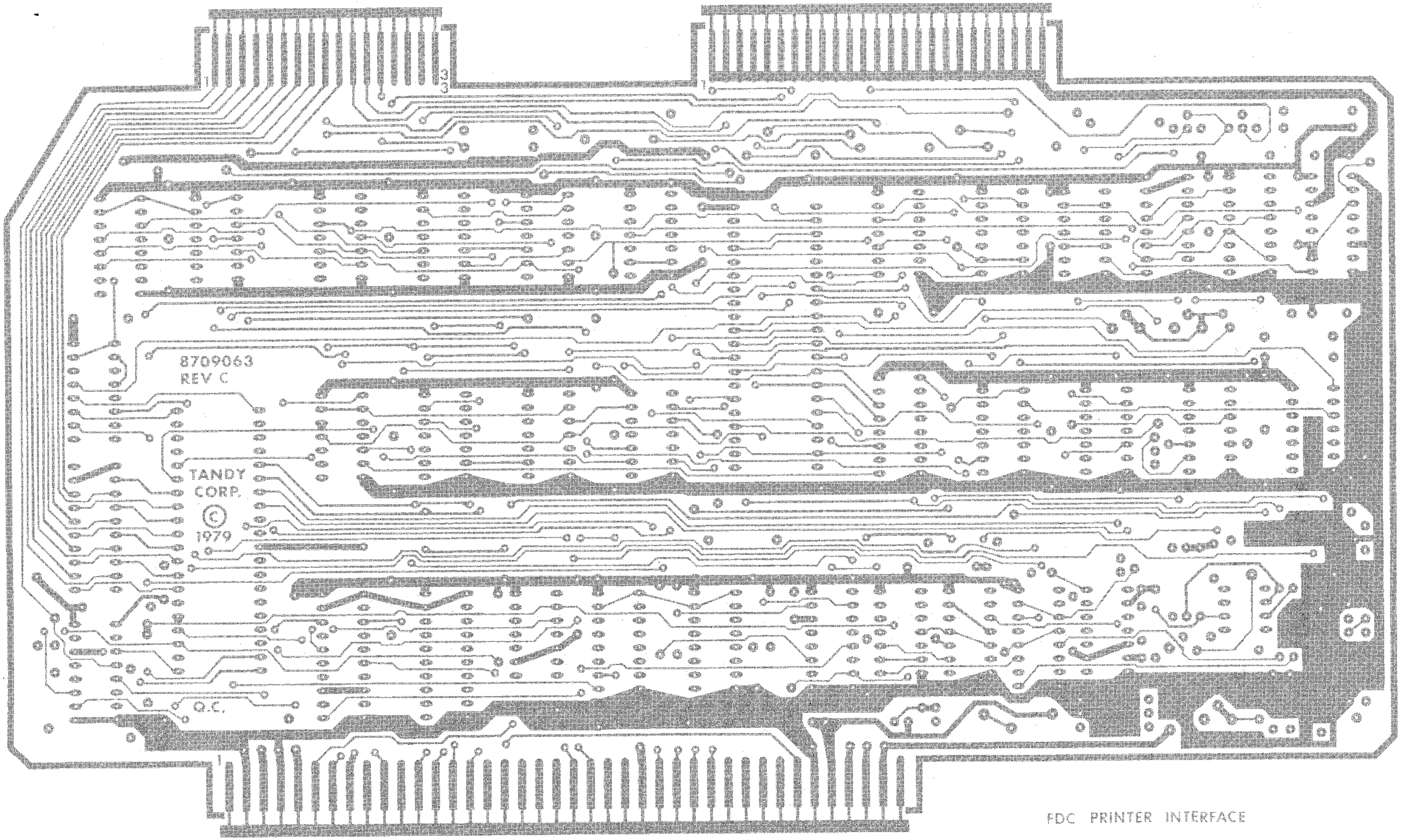


Figure 5. X-Ray View FDC Printed Circuit Board — Circuit Side

FLOPPY DISK CONTROLLER PARTS LIST

ELECTRICAL

SYMBOL	DESCRIPTION	MANUFACTURER'S PART NUMBER	RADIO SHACK PART NUMBER
	PC Board	8709063	—

CAPACITORS

SYMBOL	DESCRIPTION	MANUFACTURER'S PART NUMBER	RADIO SHACK PART NUMBER
C1	250pF, 50V, 20%, Ceramic Disc	8321251	—
C2	0.1μF, 50V, Monolithic	8374104	—
↓	↓ ↓	↓	↓
C8	0.1μF, 50V, Monolithic	8374104	—
C9	33pF, 50V, Ceramic Disc	8300334	ACC330QJCP
C10	0.1μF, 50V, Monolithic	8374104	—
C11	1300pF, 12V, 2%, Ceramic Disc	8322131	—
C12	0.1μF, 50V, Monolithic	8374104	—
↓	↓ ↓	↓	↓
C15	0.1μF, 50V, Monolithic	8374104	—
C16	0.047μF, 25V, 20%, Ceramic Disc	8323471	—
C17	0.47μF, 35V, 20%, Tantalum	8324471	—
C18	33μF, 50V, Electrolytic, Axial	8316334	ACC336QJAA
C19	33μF, 50V, Electrolytic, Axial	8316334	ACC336QJAA
C20	0.1μF, 50V, Monolithic	8374104	—
C21	0.1μF, 50V, Monolithic	8374104	—
C22	1300pF, 12V, 2%, Ceramic Disc	8322131	—
C23	0.047μF, 25V, 20%, Ceramic Disc	8323471	—
C24	110pF, 50V, 2%, Mylar	8321111	—
C25	0.001μF, 50V, 20%, Ceramic Disc	8302104	—
C26	0.1μF, 50V, Monolithic	8374104	—
C27	68μF, 35V, Tantalum, PC	8334683	—
C28	0.1μF, 50V, Monolithic	8374104	—
C29	100pF, 50V, 20%, Ceramic Disc	8321101	—
C30	33μF, 50V, Electrolytic, Axial	8316334	ACC336QJAA
C31	0.1μF, 50V, Monolithic	8374104	—
C32	0.1μF, 50V, Monolithic	8374104	—
C33	200pF, 50V, Ceramic Disc	8301204	ACC201QJCP
C34	33μF, 50V, Electrolytic, Axial	8316334	ACC336QJAA
C35	33μF, 50V, Ceramic Disc	8300334	ACC330QJCP

DIODES

SYMBOL	DESCRIPTION	MANUFACTURER'S PART NUMBER	RADIO SHACK PART NUMBER
CR1	Zener, 5.6V, 5%	8150232	ADX1350
CR2	1N4148	8150148	ADX1152
CR3	1N4148	8150148	ADX1152
CR4	1N4148	8150148	ADX1152
CR5	Zener, 6.2V, 5%	8150234	ADX1279

TRANSISTORS

SYMBOL	DESCRIPTION	MANUFACTURER'S PART NUMBER	RADIO SHACK PART NUMBER
Q1	2N2222A, NPN, TO-18 case	8110222	AMX4263
Q2	2N2907, PNP, TO-18 case	8100907	AMX4187

FLOPPY DISK CONTROLLER PARTS LIST (Cont'd)

SYMBOL	DESCRIPTION	MANUFACTURER'S PART NUMBER	RADIO SHACK PART NUMBER
	RESISTORS		
R1	2.2K, 1/4W, 5%, Carbon Film	8207222	AN0216EEC
R2	2.2K, 1/4W, 5%, Carbon Film	8207222	AN0216EEC
R3	2.2K, 1/4W, 5%, Carbon Film	8207222	AN0216EEC
R4	2.2K, 1/4W, 5%, Carbon Film	8207222	AN0216EEC
R5	50K, 10%, multi-turn potentiometer	8289350	AP7029
R6	2.2K, 1/4W, 5%, Carbon Film	8207222	AN0216EEC
R7	150 ohm, 1/4W, 5%, Carbon Film	8207115	AN0142EEC
R8	150 ohm, 1/4W, 5%, Carbon Film	8207115	AN0142EEC
R9	150 ohm, 1/4W, 5%, Carbon Film	8207115	AN0142EEC
R10	10K, 1/4W, 5%, Carbon Film	8207310	AN0281EEC
R11	150 ohm, 1/4W, 5%, Carbon Film	8207115	AN0142EEC
R12	2.2K, 1/4W, 5%, Carbon Film	8207222	AN0216EEC
R13	2.2K, 1/4W, 5%, Carbon Film	8207222	AN0216EEC
R14	10K, 1/4W, 5%, Carbon Film	8207310	ACC0281EEC
R15	2.2K, 1/4W, 5%, Carbon Film	8207222	AN0216EEC
R16	1.5K, 1/4W, 5%, Carbon Film	8207215	AN0206EEC
R17	8.2K, 1/4W, 5%, Carbon Film	8207282	AN0271EEC
R18	2.2K, 1/4W, 5%, Carbon Film	8207222	AN0216EEC
R19	2.2K, 1/4W, 5%, Carbon Film	8207222	AN0216EEC
R20	150 ohm, 1/4W, 5%, Carbon Film	8207115	AN0142EEC
R21	150 ohm, 1/4W, 5%, Carbon Film	8207115	AN0142EEC
R22	2.2K, 1/4W, 5%, Carbon Film	8207222	AN0216EEC
R23	2.2K, 1/4W, 5%, Carbon Film	8207222	AN0216EEC
R24	1.1K, 1/4W, 1%, Carbon Film	8201211	ACC0198EEC
R25	10K, 1/4W, 5%, Carbon Film	8201310	AN0281EEC
R26	270 ohm, 1/2W, 5%, Carbon Film	8217127	AN0155EFC
R27	3.48K, 1/4W, 1%, Carbon Film	8201234	AN0232BEC
R28	3.48K, 1/4W, 1%, Carbon Film	8201234	AN0232BEC
R29	5.1K, 1/4W, 5%, Carbon Film	8207251	AN0252EEC
R30	1.1K, 1/4W, 1%, Carbon Film	8201211	AN0198BEC
R31	10K, 1/4W, 1%, Carbon Film	8201310	AN0281BEC
R32	10K, 20% potentiometer	8269310	AP7028
R33	160 ohm, 1/2W, 5%, Carbon Film	8217116	AN0143EFC
R34	1.2K, 1/4W, 5%, Carbon Film	8207212	AN0196EEC
R35	1K, 1/4W, 5%, Carbon Film	8207210	AN0196EEC
R36	10K, 20% potentiometer	8269310	AP7028
R37	10K, 20% potentiometer	8269310	AP7028
R38	2.2K, 1/4W, 5%, Carbon Film	8207222	AN0216EEC
R39	2.2K, 1/4W, 5%, Carbon Film	8207222	AN0216EEC
R40	2.2K, 1/4W, 5%, Carbon Film	8207222	AN0216EEC
R41	2.2K, 1/4W, 5%, Carbon Film	8207222	AN0216EEC
R42	806 ohm, 1/4W, 1%, Carbon Film	8201180	———
R43	140 ohm, 1/4W, 1%, Carbon Film	8201114	AN0141BEC
R44	Omitted	———	———
R45	4.7K, 1/4W, 5%, Carbon Film	8207247	AN0247EEC
R46	4.7K, 1/4W, 5%, Carbon Film	8207247	AN0247EEC
R47	390K, 1/4W, 5%, Carbon Film	8207439	AN0414EEC
R48	2.2K, 1/4W, 5%, Carbon Film	8207222	AN0216EEC
R49	10K, 1/4W, 5%, Carbon Film	8207310	AN0281EEC

FLOPPY DISK CONTROLLER PARTS LIST (Cont'd)

SYMBOL	DESCRIPTION	MANUFACTURER'S PART NUMBER	RADIO SHACK PART NUMBER
	RESISTORS (Cont'd)		
R50	20K, 1/4W, 5%, Carbon Film	8207320	AN0306EEC
R51	330 ohm, 1/4W, 5%, Carbon Film	8207133	AN0159EEC
R52	2.2K, 1/4W, 5%, Carbon Film	8207222	AN0216EEC
R53	150 ohm, 1/4W, 5%, Carbon Film	8207115	AN0142EEC
R54	15K, 1/4W, 5%, Carbon Film	8207315	AN0297EEC
	INTEGRATED CIRCUITS		
U1	74LS175, Quad "D" flip-flop	8020175	AMX3566
U2	74LS153, Dual 4-to-1 line data selector/multiplexer	8020153	AMX3562
U3	74LS02, Quad 2-input NOR gate	8020002	AMX3551
U4	7416, Hex buffer	8000016	————
U5	7416, Hex buffer	8000016	————
U6	FD1791B	8045791	AXX3014
U7	74LS08, Quad 2-input AND gate	8020008	————
U8	74LS32, Quad 2-input OR gate	8020032	AMX3557
U9	74LS04, Hex inverter	8020004	AMX3552
U10	74LS08, Quad 2-input AND gate	8020008	————
U11	74LS02, Quad 2-input NOR gate	8020002	AMX3551
U12	8T26A, Bus transceiver	8060026	AMX4261
U13	74LS10, Triple 3-input NAND gate	8020010	————
U14	74LS74, Dual "D" flip-flop, positive-edge-triggered	8020074	AMX3558
U15	74LS125, Quad bus buffer with three state output	8020125	————
U16	7416, Hex buffer	8000016	————
U17	74LS174, Hex "D" flip-flop	8020174	AMX3565
U18	74LS04, Hex inverter	8020004	AMX3552
U19	74LS32, Quad 2-input OR gate	8020032	AMX3557
U20	74LS20, Dual 4-input NAND gate	8020020	AMX3555
U21	74LS32, Quad 2-input OR gate	8020032	AMX3557
U22	Z80A, PIO	8047881	AXX3015
U23	8T26A, Bus transceiver	8060026	AMX4261
U24	74LS244, Line driver	8020244	AMX3864
U25	74LS123, Dual Monostable multivibrator, retriggerable	8020123	————
U26	MC741C, Operational Amplifier	8050741	AMX4258
U27	MC4024, V.C.O.	8050024	————
U28	74S112, Dual J-K flip-flop negative-edge-triggered	8010112	————
U29	74LS74, Dual "D" flip-flop positive-edge-triggered	8020074	AMX3558
U30	74LS00, Quad 2-input NAND gate	8020000	AMX3550
U31	74LS123, Dual Monostable multivibrator, retriggerable	8020123	————
U32	8T28A, Transceiver	8060028	AMX4262
U33	8T28A, Transceiver	8060028	AMX4262
U34	7407, Hex inverter	8000007	————
U35	74LS240, Octal buffer	8020240	AMX4225
U36	74LS244, Line driver	8020244	AMX3864
U37	74LS123, Dual Monostable multivibrator, retriggerable	8020123	————
	MISCELLANEOUS		
	Plug, jumper (3)	8519021	AJ6769
	Socket, IC, 40-pin (2)	8509002	AJ6580
	Staked pins (40)	8529014	AHB9682

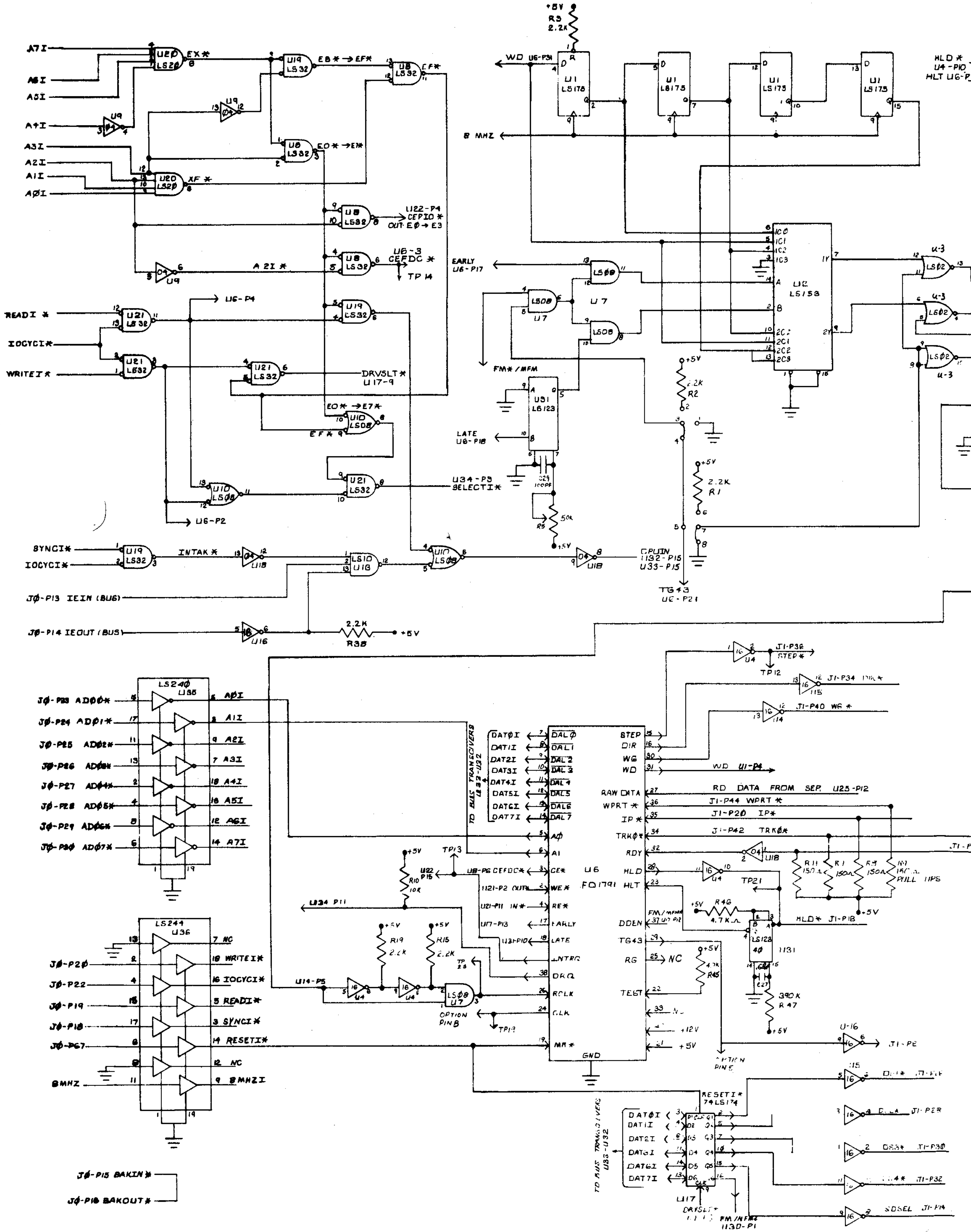
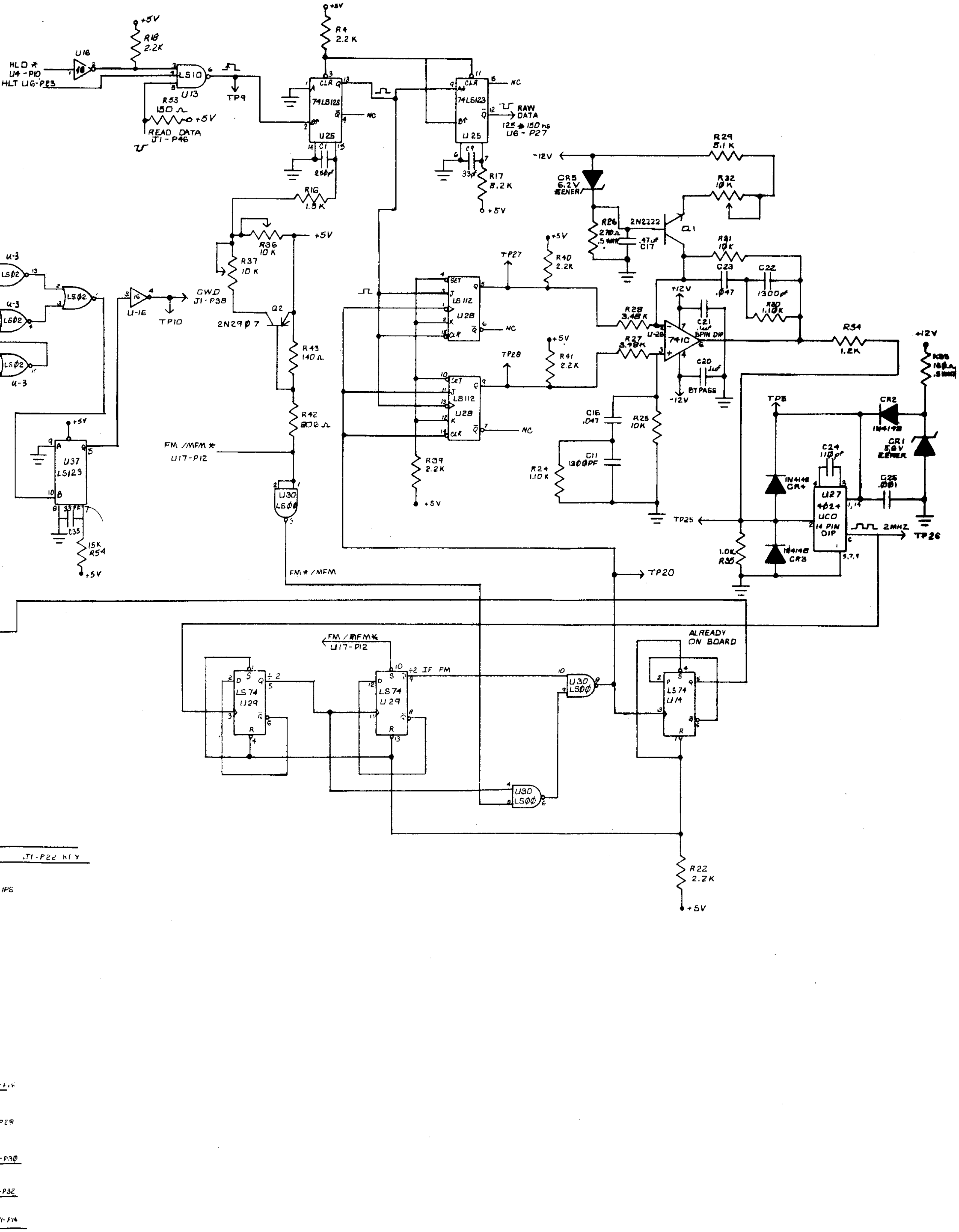


Figure 6. Floppy Disk Control



Controller Schematic Diagram — Sheet 1

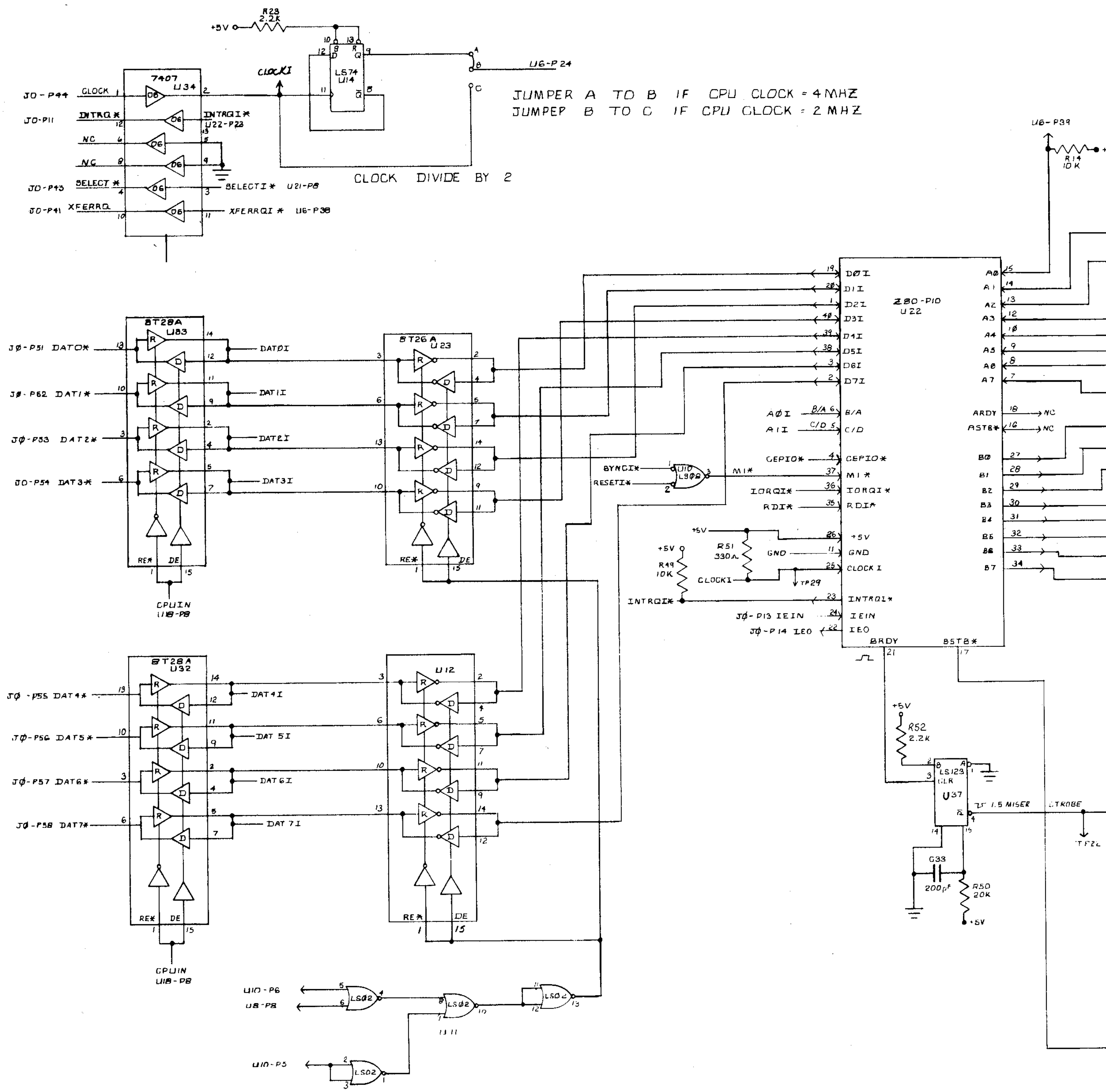
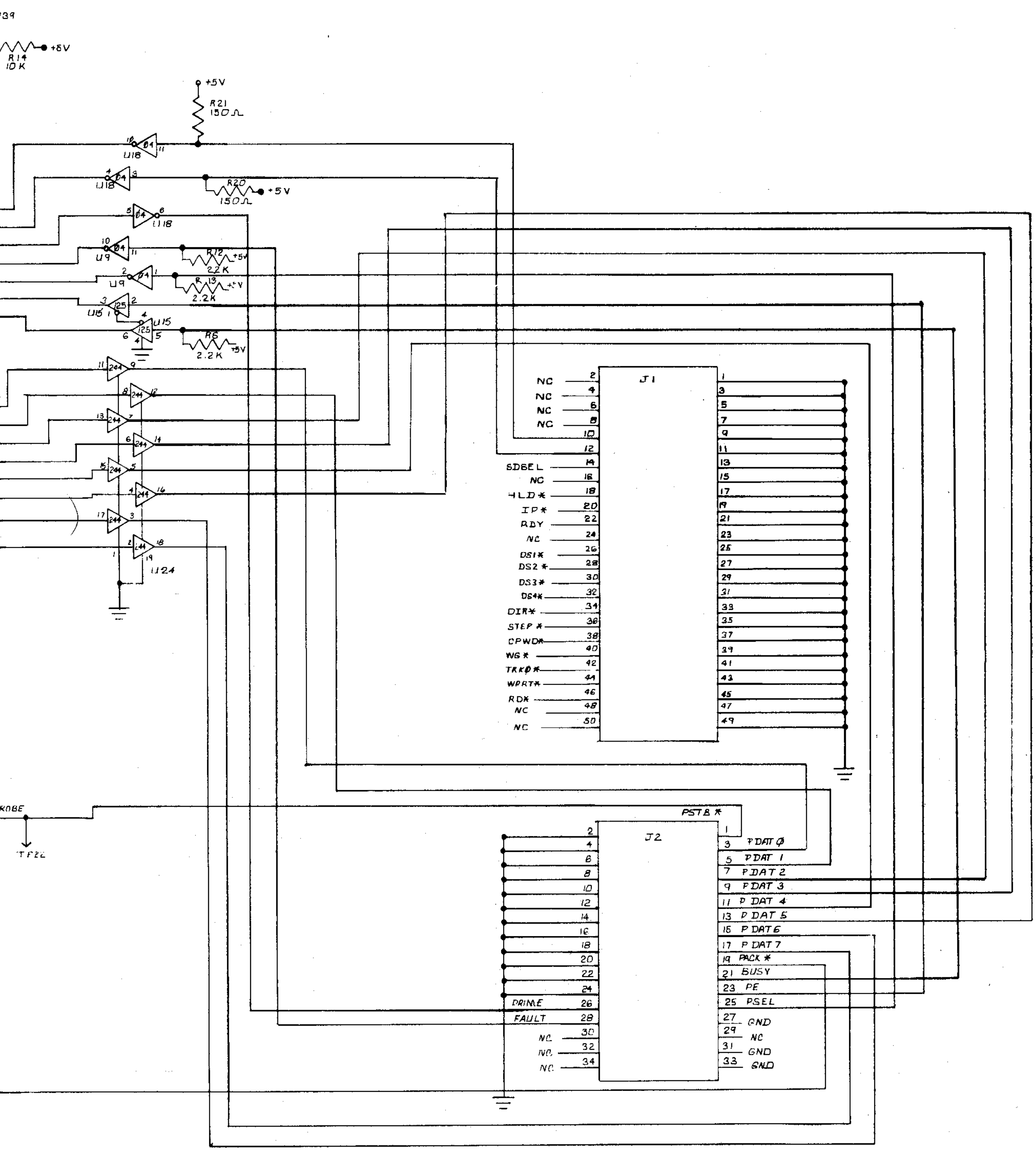


Figure 6. Floppy Disk Controller Schema



chematic Diagram — Sheet 2

SECTION V

VIDEO/KEYBOARD INTERFACE

A. FUNCTIONAL SPECIFICATIONS

The Video/Keyboard Interface board has two major functions. One is to control a built-in, 12-inch, high-resolution video monitor capable of displaying 24 lines of 80 normal characters or 40 expanded characters in both upper and lower cases. The other function is to "CONTROL" a 76-key keyboard that includes features such as "control", "escape", "hold", "repeat", and two software-programmable special function keys.

Figure 1 shows a basic block diagram of this PC Board. It includes a high speed oscillator whose frequency (12.48 MHz in this case) is the rate at which information is shifted to the CRT and dots are written; and a CRT controller providing diversified functions such as video timing and refresh memory addressing. A multiplexer switches the control of the Display RAM address bus to either the CRTC or the CPU, depending on the RAM/Video RAM Logic Selection. The system block diagram also shows a video-board select logic that controls a 3-state buffer and the keyboard control; and enables the video and the Real Time clock. Data is latched from the Display RAM into a ROM character generator, then shifted to the video output to finally appear on the display monitor.

In Figure 1, we have attempted to include as many blocks as possible, for clarity. For example, the pulse-width adjuster block (as labeled in our block diagram) is simply an MSI monostable multivibrator with schmitt-trigger inputs. Its main function is to provide noise immunity and pulse-width stability to the horizontal sync signal which is one of the CRTC outputs. Also, the Vertical sync goes through the RTC&NMIRQ* Logic to generate a Real Time clock signal (30 or 60 Hz) and a non-maskable interrupt request signal.

All these different blocks, forming our control system (Video/Keyboard), are described individually in the Theory of Operation section.

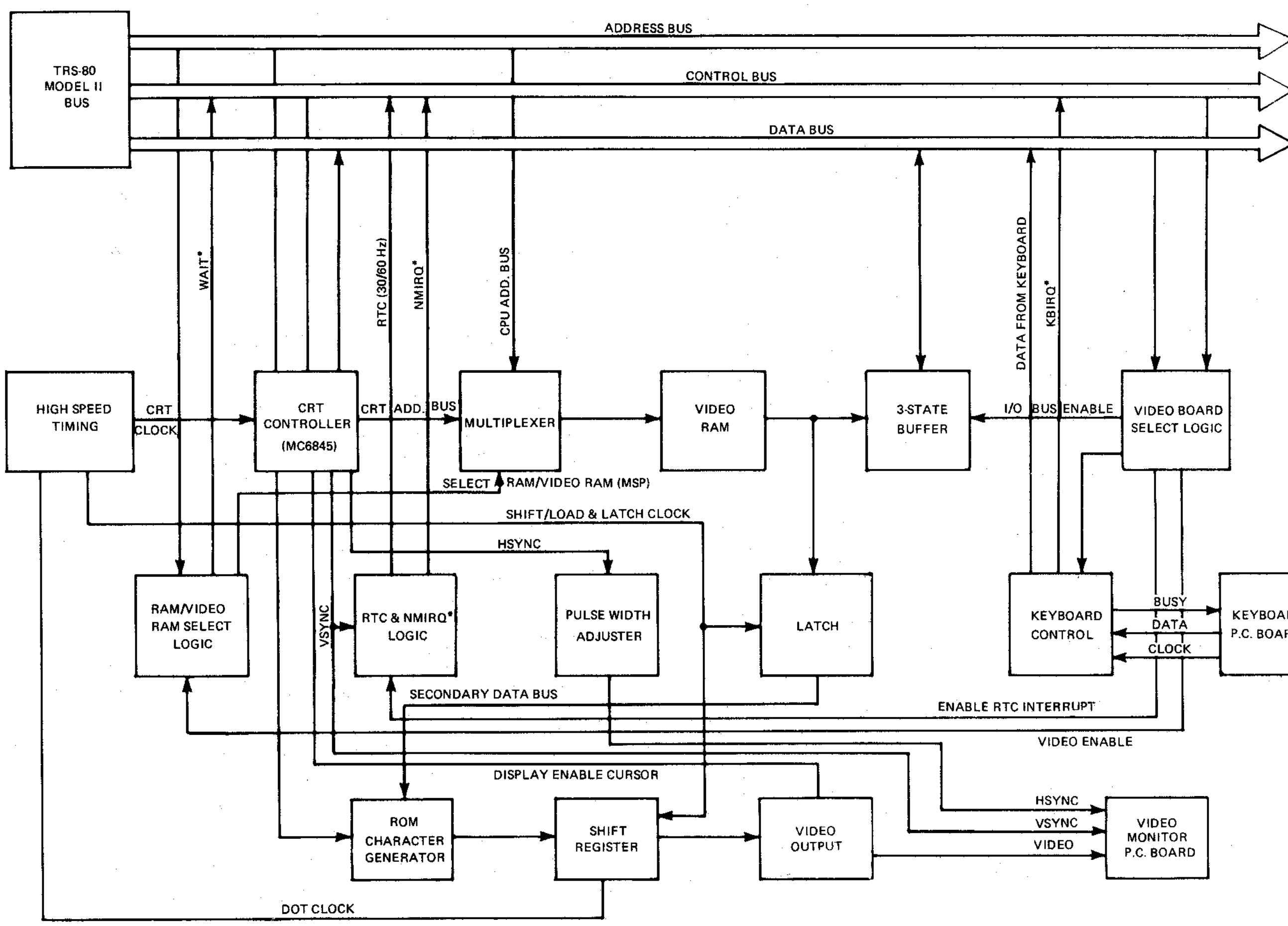


Figure 1. Block Diagram

THEORY OF OPERATION

High Speed Timing

Refer to the Video/Keyboard Schematic.

The timing for the system is derived from a dot-clock crystal oscillator. This system clock is shown in the upper left corner of the schematic. It consist of a 12.48 MHz, fundamental-cut crystal in parallel with a resonant circuit that is composed of two inverters (part of U1) that are driven into their linear region by resistors R2 and R3 (470 ohm's each).

The waveform at pin 4 of U1 resembles a "raw" square wave at about 12.48 MHz.

At pin 6 of the same chip, the signal looks more like a "clean" square wave. It is labeled RCLOCK. It goes through inverter U1 pin 9 and comes out of pin 8 as RCLOCK*. Notice that we are using the asterisk throughout the entire text as follows: if, for example, the signal RCLOCK is active high, then RCLOCK* which means "NOT RCLOCK" is active low.

At this point, that is at pin 13 of U1, RCLOCK* goes through an inverter to give RCLOCKP (RCLOCK prime) and again through a second inverter to yield RCLOCKP*. Up to this point all these clocks still have the same frequency (12.48MHz), but they are at different phases.

The reason for generating all these different clocks is that different timing is needed to synchronize the various activities of our system. That is, one activity that should take place before another, or should occur 3 or 4 times while another one happens just once. RCLOCK is divided by 2 by a "D" Flip-Flop, pins 11 and 9 of U17. That is, its frequency is halved (12.48 MHz/2 = 6.24 MHz). It is then NANDed with the 80*/40 character Enable. When this signal is low (active), 80 characters per line will be displayed on the screen; only 40 characters would appear otherwise (when high). This signal will be described in detail in later sections of the text.

CLOCK, at pin 8 of LSØØ (test point 26, TP26), is at either 12.48 MHz (for 80 characters) or at 6.24 MHz (for 40 characters). Note that the NAND gate, U28 (pins 1, 2, and 3), is used here as an inverter. CLOCK goes through inverter U33 (pins 11 and 10) to become DCLK, which is the DOT CLOCK. Its frequency (either 6.24 or 12.48 MHz) is the rate at which information is shifted to the CRT and dots are written.

CLOCK, which is a phase shifted DOT CLOCK, is divided down by a 4-bit counter (U26) to produce the character-rate clock labeled here as CCLK with a frequency of 12.48/8=1.56MHz (for 80 characters) or 6.24/8=0.78MHz (40 characters).

This 4-bit counter (LS163) is synchronous. That is, all its Flip-Flops are clocked simultaneously so that the outputs change coincident with each other when instructed by the count-enable inputs and internal gating. The DOT CLOCK triggers the four Flip-Flops on the rising edge of its wave form. The count is done as follows: (in HEX)
Ø, 9, A, B, C, D, E, F, Ø, 9, A, B, C, . . . etc. This is best described by the Timing diagrams of Figure 2. Notice that both 80 and 40 character modes are represented here. Also the signals TCLK* and PLCLK* are shown on these Timing diagrams.

These diagrams are fairly reliable for comprehension purposes since the propagation delay times, due to the different gates, were not neglected.

We need all these different signals because each of these signals is doing its own "specific job" just like any member in a working team.

How? Well, for example the CCLK triggers the MC6845 CRT controller which, if enabled, would send an address to the video RAM requesting data to be sent to the Latch (U8) inputs. TCLK* will then latch it into the character ROM, which at its turn would send the appropriate dots to the shift register U10. PLCLK* will shift load them in a parallel fashion into the 8-bit shift register (U10) and DCLK will shift them out of it serially toward the Video.

Further explanation of the different parts of the system that need to be clocked will provide more clarity to this subject of Timing Coordination. One of these parts is the CRT controller.

Cathode Ray Tube Controller (CRTC)

For our video monitor display, we are using the Motorola Controller MC6845, a reliable processor that controls the monitor with no CPU intervention, until the video memory receives new data to be processed.

The MC6845 simplifies not only the design and the architecture, but also the trouble-shooting of the video control board. It sharply reduces the number of I.C. chips it would have taken otherwise. This CRTC commands the interface to raster scan CRT displays. It also provides video timing and refresh memory addressing. The CRTC is a collection of registers, counters and comparators that time all logic activities as the interfaced raster scan proceeds. Its logic consists of programmable horizontal and vertical timing generators, linear register, cursor logic, light-pen capture register and control circuitry for interfacing to a processor bus. The CRTC permits easy timing and synchronization of signals. It also handles raster graphics as well as alphanumeric applications.

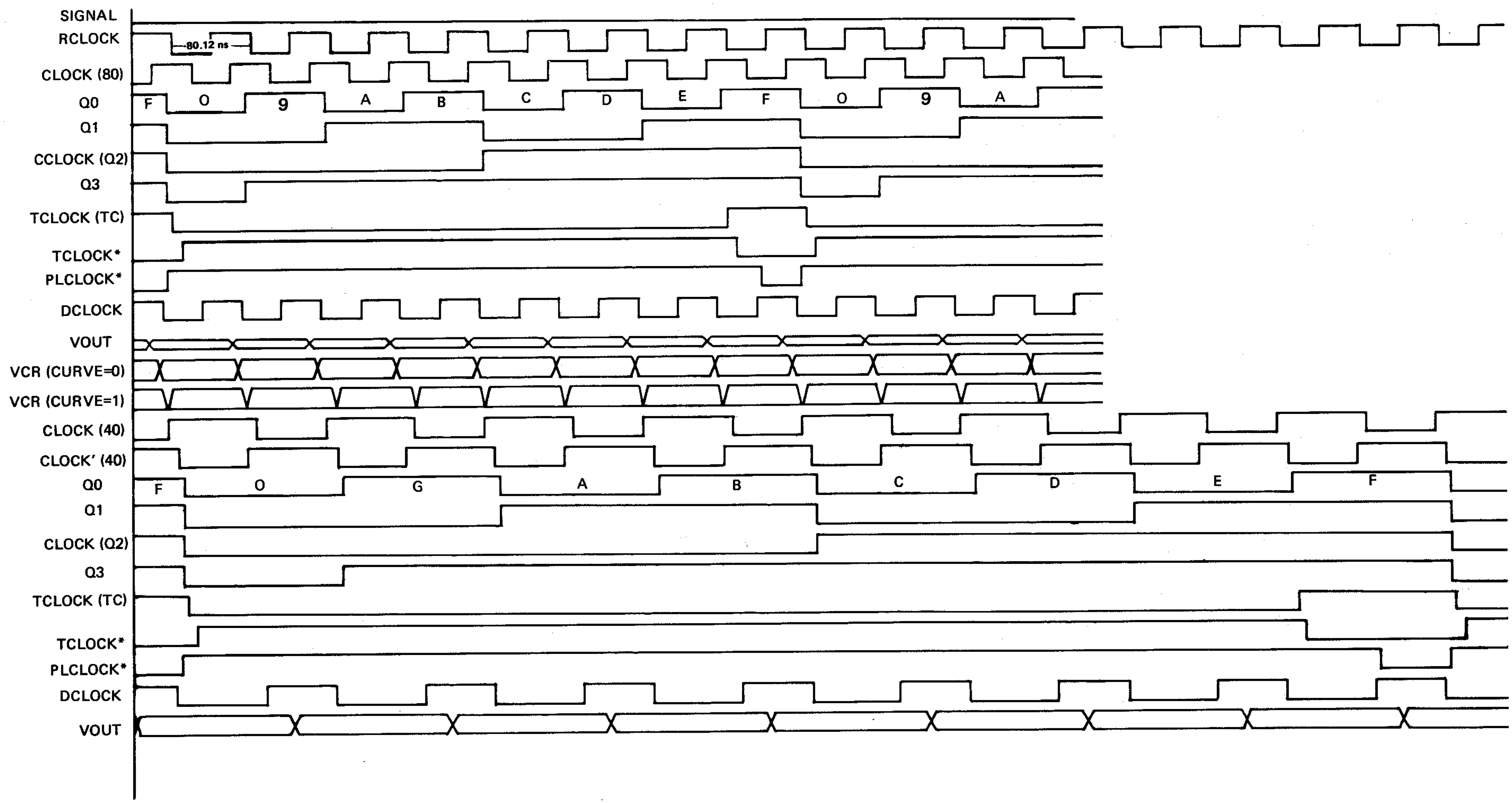


Figure 2. Timing Diagrams

It is fully programmable through the CPU data bus, thus generating timing for almost any alphanumeric screen density. Therefore it is up to the designer to choose any screen density he or she wants. That is 80X24, 132X20, etc.

For example in our case we are using 80X24 and 40X24. That is, 24 lines with 80 alphanumeric characters each (for the 80 character mode) and 24 lines with 40 alphanumeric characters each (for the 40 character mode). One can set this screen density by programming the registers of the CRTC. The CPU communicates with the CRT controller through a buffered 8-bit data bus by Reading or Writing into the 18 registers of the CRTC.

One primary function of this CRT controller is to generate refresh addresses, row addresses, video monitor timing (horizontal and vertical sync), cursor and display enable.

The best way of describing this MC6845 controller is to refer to the pin description as explained in the Motorola microcomputer data library. The following is a description of every pin of the CRTC chip. The MC6845 controller is labeled in the schematics as U11 and is redrawn below in Figure 3.

1. Processor Interface:

The CRTC interfaces to the processor bus on the bidirectional data bus (DØ-D7) using CS*, RS, E and R/W* for control signals. The data bus lines (DØ-D7) are used for Data transfers between the CRTC internal register file and the processor.

The enable signal (pin 23) of U11 is a high impedance TTL/MOS compatible input which enables the data bus input/output buffers and clocks data to and from the CRTC. In our schematics the CRTC is enabled by either the RD* or WR* (U42 pins 11, 12 & 13). The high to low transition is its active edge.

The chip select (CS*) when low, selects the CRTC to read or write the internal register file. It is active (low) only when there is a valid stable address being decoded from the processor. In our case it is active when either I/O port FC* or FD* is active (U31, pins 7 and 6). The register select line (RS) is an input which selects either the address register (RS = Ø) or one of the data registers (RS = 1) of the internal register file.

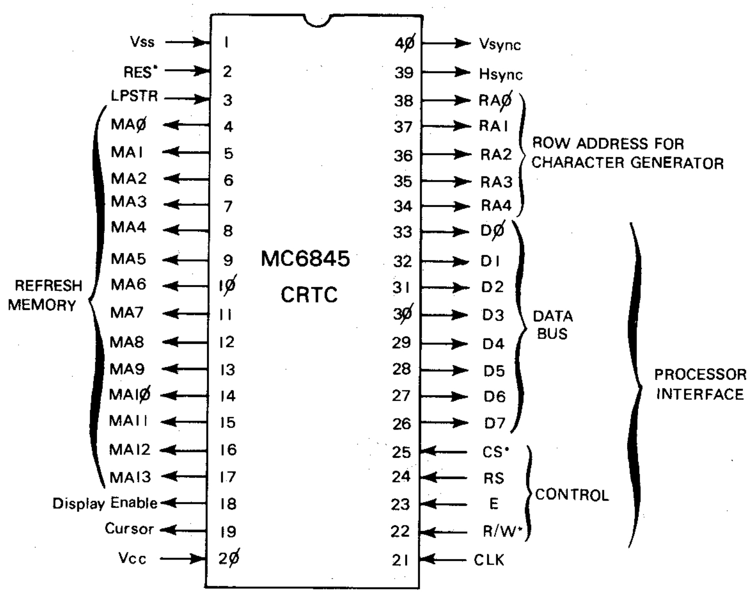


Figure 3. MC6845 – Pin Identification

The Read/Write (R/W*) signal determines whether the internal register file gets written or read. It is written when low and read when high.

2. CRT Control:

The CRTC provides Horizontal Sync (HS), Vertical Sync (VS) and Display Enable signals.

The Vertical Sync is an active high signal which drives the monitor. It determines the vertical position of the displayed data. The Horizontal Sync is also an active high signal which drives the monitor. It determines the horizontal position of the displayed data.

The Display Enable is an active high signal which indicates the CRTC is providing addressing in the active display area.

3. Refresh Memory/Character Generator Addressing:

The CRTC provides Memory addresses (MAØ-MA13) which scan the Refresh RAM. In our case only MAØ through MA1Ø are used, since our video memory capacity is only 2K bytes big. Also provided are Raster addresses (RAØ-RA4) for the character ROM. The Refresh Memory addresses (MAØ-MA1Ø) are used to refresh the CRT screen with pages of data located in the 2K block of Display RAM.

The Raster addresses (RAØ-RA4) determine the row of a character in the character ROM.

4. Other Pins:

The clock input is used to synchronize all CRT control signals. In our design this signal is the character-rate clock CCLK (1.56/0.78 MHz). The active transition is high to low.

The Light Pen Strobe (LPSTR) is not used in our design. The cursor, which is an active high signal, indicates cursor display to external video processing logic.

The Reset (RES*) input is used to reset the CRTC. It is active low. When this signal is active, the CRTC is forced into the following status:

a) All the counters in CRTC are cleared and the device stops the display operation.

b) All the outputs go down to low level.

c) The control registers of the CRTC are not affected.

Now that we have an overview of the CRTC chip itself, let's try to clarify what is meant by memory refreshing. The way we programmed our CRTC internal register file would permit a display of 24X80/24X40 alphanumeric characters. The address of each one of these characters is stored in the display memory. That is the reason we are using only 2K of Video RAM (just enough to store the entire screen density).

As you may know, everything that is displayed on the screen should be continuously refreshed, otherwise it will fade away and disappear. Every character is a dot matrix of 8x10 cells and every cell is refreshed about 60 times in one second. (Refer to Figure 4.) The CRT beam is repetitively scanning the screen from top to bottom, refreshing every dot whose location is indicated by the coordinates that the display memory and the character ROM receive from the CRTC (Memory refresh address and Row address).

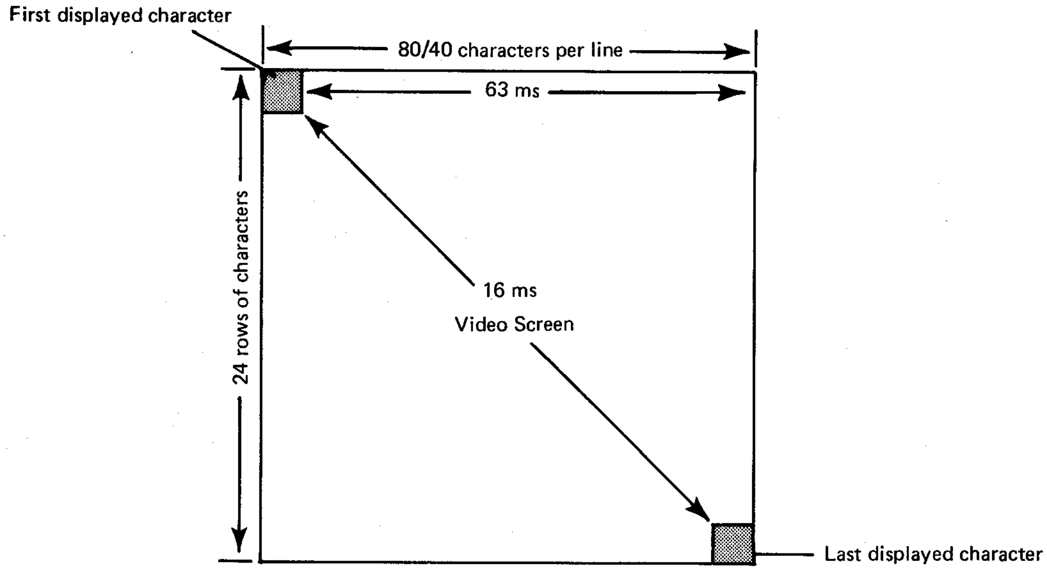
The CRTC takes care of this particular chore and the CPU would therefore do a more "smart" activity, rather than waste its "valuable" time with this refreshing routine. However, everytime the CPU addresses its upper 2K bytes of memory, it automatically takes control of the Video RAM. The reason is that these 2K bytes, starting at address locations F8ØØH through FFFFH, overlap the video memory in its entirety. Thus this display RAM can be accessed by either the CPU or the CRTC, but not by both at the same time.

Our approach for solving contentions for the refresh memory is that the processor (CPU) gets priority access anytime, but is synchronized by an interrupt to perform accesses only during the vertical retrace time. The vertical retrace time is defined as the time it takes the CRT beam to return from the end of the very last scan line, back to the start of the very first one. Of course the CRT beam is shut off during the retrace time.

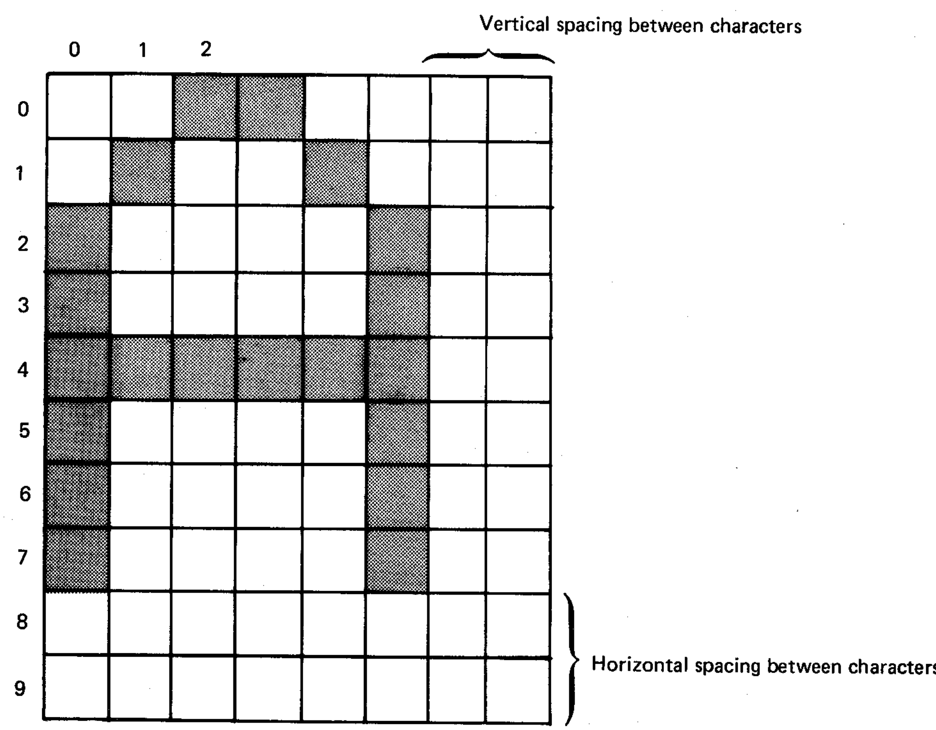
The CRTC sends its addresses as follows: The first set of address lines consisting of MAØ through MA1Ø, cycles binarily through the display memory and is incremented with each clock pulse (CCLK); one per character displayed. The second set (RAØ-RA4) addresses the row-address select lines of the character generator. These also cycle binarily, but are incremented with each horizontal retrace time. Again the horizontal retrace time is the period in which the CRT beam returns from the end of a scan line back to the beginning of the next one.

The CRTC's linear address generator repeats the same sequence of character addresses for each scan line within the same character row.

The character block in our case is 10 rows high, so it takes 10 separate accesses of a given character to write its 10 dot-rows on the screen. So putting 80X24, or 1920, characters on the screen calls for 10X1920, or 19200, character accesses 60 times every second.



Video screen density: 80/40 x 24 characters.
Only $(1920)_{10}$ locations are displayed of the 2K Ram contents.



ONE CHARACTER LOCATION (Example of the upper case letter A)

Figure 4. Character Dot Pattern

Multiplexers

As you can see in the schematics, LS157 multiplexers (U23, U24 and U25), are used for multiplexing refresh memory addresses between the processor and the CRTC.

The processor is in control when the select inputs (pin 1 of each chip) are high. When these inputs are low the control of the display is switched to the CRTC.

MSP, the signal that controls the multiplexing is derived from the RAM/VIDEO RAM Select Logic block.

RAM/Video RAM Select Logic

The block, labeled RAM/VIDEO RAM Select Logic, on the diagram of Figure 1, is actually a sort of decoder. That is, when the CPU is addressing its upper 2K bytes of memory, located at F8ØØH through FFFFH, address lines AD11 through AD15 become high (active). Also the Memory request signal or memory cycle (MEMCYC) is activated by the CPU. As you may know by now, this signal is activated everytime the CPU addresses any part of its memory. Another important signal is the input to pin 11 of NAND gate LS30, U41. This signal is used to enable the CPU to access the Video RAM if, and only if, our software says so. That time is when Port FFWR* is activated and bit 7 (D2 of LS175) is set to 1. If all these conditions are met, then pin 8 of U41 goes low and MSEL becomes high (U30 pin 6).

MSEL is ANDed with MSLP (U13 pins 4, 5 & 6) to finally give us MSP, the select input to the multiplexers. When this MSP signal is high, the Video RAM is under the processor control. Note that when the Reset* button is hit (U32 pin 8), the CPU loses that control (MSP becomes low).

The refresh cycle, that is the period in which the CRT beam is "within the screen", is additionally protected by the generation of a wait cycle. As is shown on the schematics, MSEL* clocks a high (U32 pin 15) that is inverted by U14 pins 2 and 3 to give an active WAIT* state. This WAIT* state is interrupted whenever we have a RESET* or MSELP NANDed with Q, as shown by U2 pins 8, 9, 10, and U29 pins 8, 9, and 10. Note that when MSELP is high, the CPU is accepting the diaplay RAM (U13 pins 4, 5, and 6).

Video Board Select Logic

This part of our system could be called the port addressing block.

It is using the lower eight lines of the address bus, as shown by U27 LS30, for the dual 2 to 4 line decoder (U31 LS155). One of the decoders is enabled only by Read NANDed with I/O Cycle signal (IOCYC) to give 3 Read ports (FCRD*, FERD*, and FFRD*; pins 9, 11, and 12). The other is enabled only by the IOCYC signal and its outputs could actually be used for Read or Write ports. In our design either one of the FC* or FD* ports could chip select the MC6845 controller. Port FF* NANDed with WR* gives FFWR* (U3 pins 8, 9, and 10). Also the Input/Output address select (U27 pin 8 and U30 pins 12 and 13) is ANDed with IOCYC to give the I/O Select (IOSEL) to enable the 3-state buffers (U34 and U35) to either Read from the CRTC (IOBIE: I/O Bus Input Enable) or Write into it (IOBIE*: I/O Bus Output Enable). Note that test points TP22 (U13 pin 3) and TP21 (U2 pin3) will show us if we are reading from or writing into the CRTC. The following table shows the port addressing and the functions of every port.

Table 1. Port Addressing

PORT ADDR.	READ FUNCTION	WRITE FUNCTION
FC	Read Keyboard data Clear Keyboard Interrupt	Load CRTC address Register
FD	Read CRTC Data Register	Load CRTC data Register
FE	Clear Real Time clock (RTC) interrupt	
FF	Read Non-maskable Interrupt Register and Non-maskable Interrupt Mask Register.	Load Memory Bank Select Register and load Non-maskable Interrupt Mask Register and Video enable.

For Example, Port FF is used as follows:

a) Non-maskable Interrupt Mask Register and Bank Select Register: Write only

D7 D6 D5 D4 D3 D2 D1 DØ

Bit 7 (D7)

– if set (1), enables the 2K bytes RAM, disables the upper 2K bytes of the Bank's RAM (F8ØØH to FFFFH)

– if Reset (Ø), disables Video RAM, enables Bank RAM F8ØØH to FFFFH.

Bit 6 (D6)

– if Ø, enables Video display (on)
– if 1, Video display off

Bit 5 (D5)

– Set (1), enables the Real Time clock (RTC) interrupt
– Reset (Ø), disables the RTC interrupts

Bit 4 (D4)

– 1, enables the 40 character mode and disables the 80 character mode
– Ø, enables the 80 character mode, disables the 40 character mode

Bits 3 through Ø (D3 - DØ)

– Selects 1 of 16 memory banks. Note that if we hit the Reset, the RTC interrupt is disabled

b) Non-maskable Interrupt Mask Register:
Read only

D7 D6 D5 D4 D3 D2 D1 DØ

- D4 — 80*/40 character mode
- D5 — RTC interrupt enable
- D6 — Video display enable*
- D7 — Keyboard Interrupt Request (KBIRQ)

Bit 7 (D7)

– 1, Keyboard interrupting
– Ø, No Keyboard interrupting

Bit 6 (D6)

– 1, Video Display disabled
– Ø, Video Display enabled

Bit 5 (D5)

– RTC interrupt enable

Bit 4 (D4)

– 80*/40 character mode*

Bits 3 through Ø (D3 - DØ)

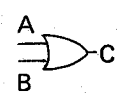
– They are "don't care" bits (not used)

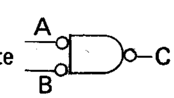
Now that we know how these different ports will be used, we can set the control bits, say in Port FF, the way we want to. This means we will be writing into Port FF. Therefore the FFWR* signal is activated. If, for example, we set bit 7 to 1, bit 6 to Ø, bit 5 to 1 and bit 4 to Ø, FFWR* will latch this data vector into our system and the following results will be obtained:

Pin 11 of U41 will be high, thus enabling the 2K byte Video RAM. BLNKVID*, Q3 (pin 14 of U18) will go high and disable the blank Video (Video on).

The Real Time clock (RTC), pin 3 of U18, is enabled. And finally we will get a low (Ø) at pin 7 of U18. This generated signal is what we previously called the 80*/40 character mode. In this case the 80* character mode is enabled (low). It is inverted at U30 pins 1, 2, and 3 and then NANDed with RCLOCK* to appear at the output of the NAND gate U28, pins 8, 9, and 10, as CLOCK (TP26).

Note how the OR gate U3 pins 4, 5, and 6 is drawn as a NAND gate.

This gate 

is the same as this gate 

We sometimes show the OR gates as above, because we are using mostly active low signals. We can go from one gate to another just by using DeMorgan's Theorem. For the above example, we have:

$$\overline{\overline{A}\,\overline{B}} = \overline{\overline{A}} + \overline{\overline{B}} = A + B = C$$

Now if we want to Read the Status of Port FF, we'll activate the FFRD* signal to enable the 3-state buffers LS240, U38. This will produce the status of the KBIRQ*, the BLNKVID*, the 80*/40 character mode* and the ENABLE RTC INT* as shown at the inputs 2, 4, 6 and 8 of U38.

Other Blocks

The 3-state Buffers (U37) are enabled by either the Video Read (VRD) or Video Write* (VWR*). VRD is the result of the RD signal ANDed with MSP (U13 pins 11, 12, and 13). VWR* is the output of WR NANDed with MSP (U2 pins 4, 5, and 6).

When the CPU wants to write data into the Video RAM, VWR* goes low (pin 1 of U37). When it does a reading from the Video RAM, VRD (high) is active (pin 15 of U37). Test points TP2 and TP24 will help us detect if data is read from or written into the Display RAM by the CPU.

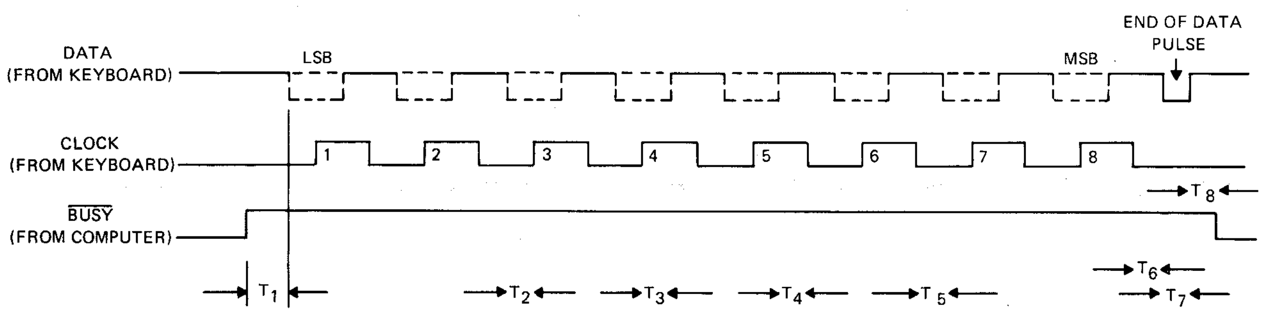
The keyboard control consists of an LS74 Flip-Flop (U17 pins 2, 3, and 5) showing the keyboard mode. That is, when data is being clocked in from the keyboard, a busy signal is sent to the system bus at the end of every word (8 bits of data). A busy (active low) signal goes from pin 5 of U17, back to the keyboard processor telling it to stop sending data. Also the same signal goes toward the CPU under the name of Keyboard Interrupt Request (KBIRQ*), telling it that a word of data is ready to be read. Data is clocked serially out of the keyboard into the shift register (U6), and then latched into the system data bus when FCRD* port is activated. Note that when FCRD* is activated (low), the Flip-Flop U17, pins 2 and 3) becomes set and the KBIRQ* or BUSY* signal goes high (disable). Now that the keyboard logic does not receive the active busy signal, it will start sending data again.

The timing diagram of Figure 5 shows how data is leaving the keyboard in the serial fashion. Notice the narrower pulse labeled End of Data pulse. It is generated at the end of an 8 data bit sequence. Its rising edge latches a low to the output of U17 pin 5. This low signal (KBIRQ* or BUSY*) informs the CPU that a word is ready to be read. It also prevents the keyboard from sending more data until the actual 8 bit word at the output of the shift register (U6) is buffered into the data bus (in other words, read by the CPU).

The RTC and NMIRQ* logic block takes the VSYNC signal, divides it by 2 (U16 pins 2, 3, 5, and 6) to yield a 30 Hz RTC. The 60/30 Hz RTC signal clocks a high into the output of U16 pin 9 to generate an RTC interrupt (RTC INT) signal which is ANDed with ENABLE RTC INT (U29 pins 12 and 13). The output of U29 (pin 11) is then inverted and goes to the system bus as a Non-maskable Interrupt Request (NMIRQ*). Note that we can clear this NMIRQ* signal by activating Port FERD* (Flip-Flop U16 pin 13).

The pulse-width adjuster is as defined in the earlier section of this text. It consists of a monostable multivibrator with schmitt-trigger inputs that provide noise immunity and pulse-width stability to the horizontal sync signal (U5, 74121). The remaining parts of the system block diagram, such as the Latch, the character ROM, the Shift Register, etc. . . . can be better defined by "tracing" the data path as follows:

The CPU writes a word of data into the Video RAM. The CRT controller, which automatically displays the Video RAM contents on the Video screen, moves that word and stores it temporarily in the Latch. The Latch will retain the byte for processing so that the RAM can get ready to send the next byte.



T_1 10µs MIN	T_5 1µs MIN
T_2 1µs MIN	T_6 1µs MIN
T_3 1µs MIN	T_7 1µs MIN
T_4 1µs MIN	T_8 1µs MAX

Figure 5. Keyboard Timing Diagram

The Latch (U8) is an LS273. When activated (by TCLK*), U8 would latch the data word into the character ROM (U9) in ASCII form. Note that the 8th bit is used as a Reverse Video signal (REVID). U9 is the character generator. The seven bit ASCII Word applied to its inputs would address a certain area in it. These ASCII inputs are considered the higher seven bits of an address. The lower part of the address comes from the CRTC (RAØ-RA4). This lower part selects the row position of the addressed dot pattern.

Each character consists of a dot matrix, 8 dots wide and 10 dots deep. Since each character consists of a pattern of dots, there must be some method to determine which dot should be on and which dot should be off to form any one character. The character generator controls the dot patterns on the screen.

U9 outputs 8 dots (on or off) at the same time. RAØ through RA4 would of course select the row of the addressed pattern. The character generator must output 10 times to build one character.

Here is how a typical character line is written:
Assume an ASCII word is in the Latch. The electron beam is on the first scan line of the character. Hence, the row address is binary "Ø". That is, RAØ through RA4 are low. U9 outputs the first dot pattern for that particular ASCII character. The next ASCII character is applied to U9. At the same time, the row address is incremented. It is now binary "1" pointing to the second scan line. Keep in mind that the electron beam doesn't stop at the last dot of the first pattern, but goes on scanning the rest of the entire scan line. By the time the second dot pattern goes out, the third ASCII word comes in. This process goes on until the entire character (10 rows) is written on the screen.

These various dot patterns are loaded into the shift register U10, in a parallel fashion and are shifted out of it serially. Of course all this is done so fast that it seems that the entire character is displayed not "in pieces" but as an entity. After the eight dot scans are outputted, the electron beam is turned off and two rows (the 9th and 10th) of blank dots are outputted. We now are ready to output the first row of the second character line. Following the path data goes through before being outputted at pin 9 of U10 (V out), one can see that the V out signal is delayed quite a bit with respect to the Display Enable and Cursor signals. For this reason, these two signals are delayed by two TADCLK cycles and Reverse Video (REVID) is delayed by one TADCLK cycle with respect to the VOUT signal. This is shown by U12. Note how the delayed cursor and DREVID are Exclusive ORed (U4 pins 12 and 13). The resulting signal at pin 11 of U4 is also Exclusive ORed with VOUT (U4 pins 9 and 10).

This is to say that either the cursor, the Reverse Video or the Video would be displayed in a character location, but not two of them at the same time. The signal outputted at pin 8 of U4 is finally enabled by the Display enable and either one of the RCLOCK, RCLOCK*, RCLOCKP and RCLOCKP* signals. We gave ourselves the option of choosing one of the four clock signals to achieve a better result. The final signal we get at pin 12 of U15 is what we simply call VIDEO. The VIDEO, HSYNC, and VSYNC signals are separately shielded and sent to the CRT Logic board. (Ground signals are wrapped around them.)

CONNECTOR J2 SIGNAL DESCRIPTIONS

PIN	SIGNAL DESCRIPTION
1	Data from Keyboard
2	Key - No Connection
3	Clock from Keyboard
4	Busy to Keyboard
5	+5V to Keyboard
6	Ground to Keyboard

CONNECTOR J3 SIGNAL DESCRIPTIONS

PIN	SIGNAL NAME	DESCRIPTION
1	HS GND	Horizontal Synchronization Ground
2	VS GND	Vertical Synchronization Ground
3	HSYNC'	Horizontal Synchronization (prime)
4	VSYNC'	Vertical Synchronization (prime)
5	KEY	No Connection
6	VIDEO	Video Signal
7	VID GND	Video Ground

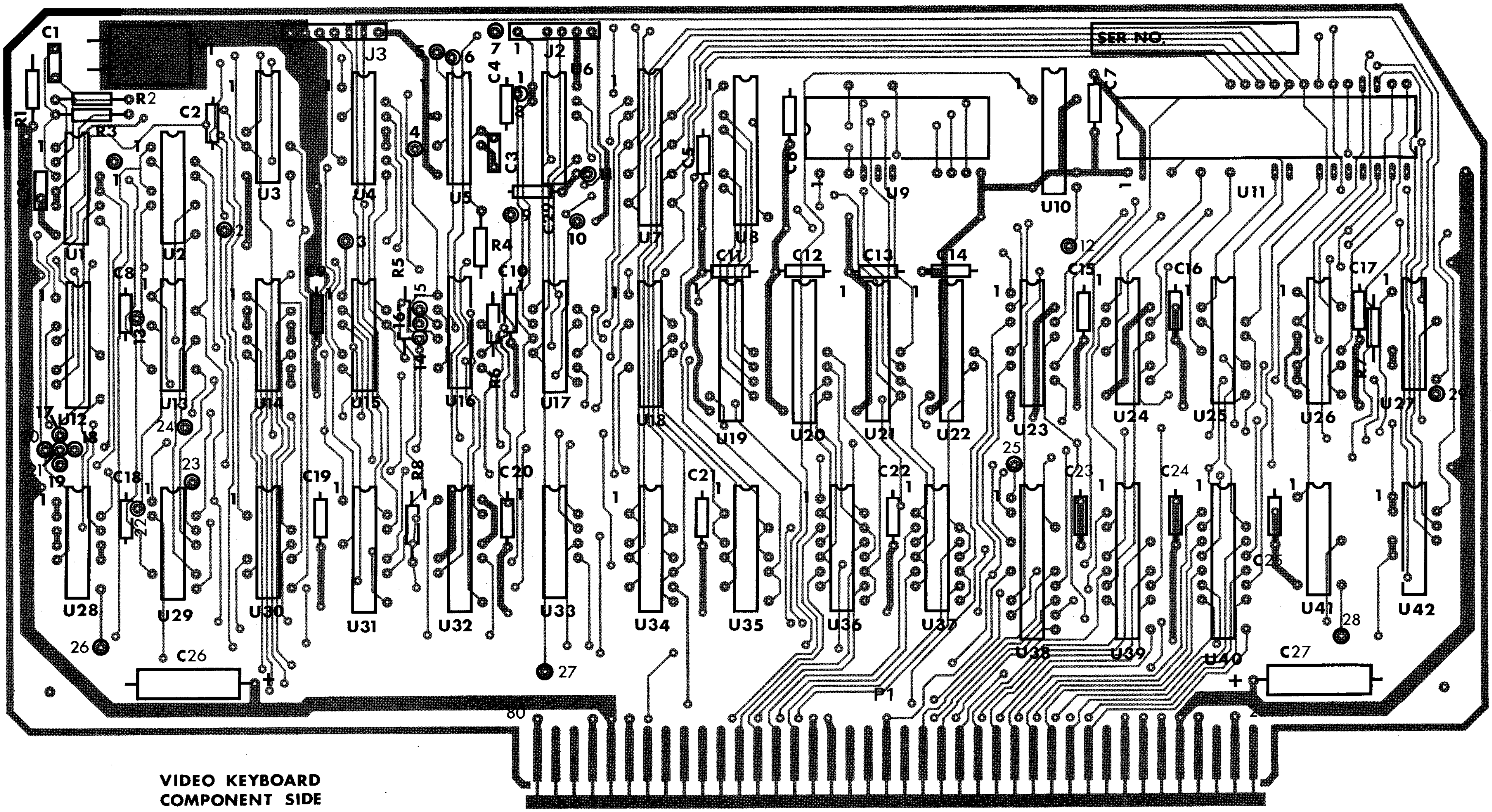
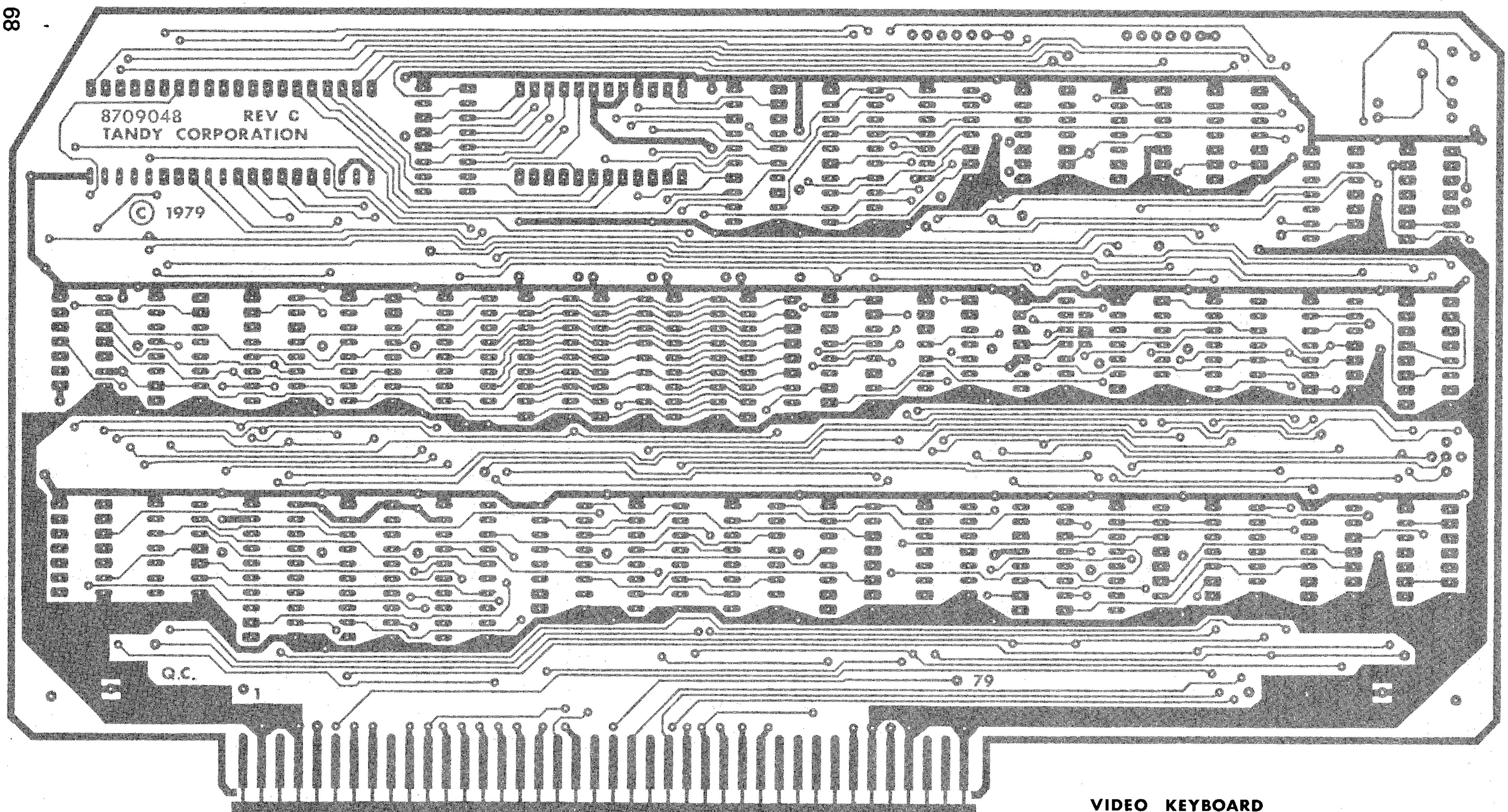


Figure 6. X-Ray View Video Keyboard Printed Circuit Board — Component Side



VIDEO KEYBOARD
SOLDER SIDE

Figure 7. X-Ray View Video Keyboard Printed Circuit Board – Circuit Side

VIDEO/KEYBOARD INTERFACE BOARD PARTS LIST

SYMBOL	DESCRIPTION	MANUFACTURER'S PART NUMBER	RADIO SHACK PART NUMBER
	ELECTRICAL		
	PC Board	8709048	————
	CAPACITORS		
C1	0.01μF, 25V, Ceramic Disc	8303102	ACC103QFCP
C2	0.1μF, 50V, Monolithic	8374104	————
C3	1000pF, 50V, Ceramic Disc	8302104	ACC102QJCP
C4	0.1μF, 50V, Monolithic	8374104	————
↓	↓ ↓	↓	↓
C25	0.1μF, 50V, Monolithic	8374104	————
C26	33μF, 50V, Electrolytic, Axial	8316334	ACC336QJAA
C27	33μF, 50V, Electrolytic, Axial	8316334	ACC336QJAA
C28	15pF, 50V, Ceramic Disc	8300154	ACC150QJCP
C29	150pF, 50V, Ceramic Disc	8301154	ACC151QJCP
	CONNECTORS		
J2	6-pin right angle	8519017	AJ6765
J3	7-pin right angle	8519022	AJ6770
	RESISTORS		
R1	4.7K, 1/4W, 5%, Carbon Film	8207247	AN0247EEC
R2	470 ohm, 1/4W, 5%, Carbon Film	8207147	AN0169EEC
R3	470 ohm, 1/4W, 5%, Carbon Film	8207147	AN0169EEC
R4	39K, 1/4W, 5%, Carbon Film	8207339	AN0330EEC
R5	4.7K, 1/4W, 5%, Carbon Film	8207247	AN0247EEC
R6	4.7K, 1/4W, 5%, Carbon Film	8207247	AN0247EEC
R7	4.7K, 1/4W, 5%, Carbon Film	8207247	AN0247EEC
R8	4.7K, 1/4W, 5%, Carbon Film	8207247	AN0247EEC
	CRYSTAL		
Y1	12.48 MHz	8409004	AMX2570
	INTEGRATED CIRCUITS		
U1	74LS04, Hex inverter	8020004	AMX3552
U2	74LS00, Quad 2-input NAND gate	8020000	AMX3550
U3	74LS32, Quad 2-input OR gate	8020032	AMX3557
U4	74LS86, Quad 2-input exclusive OR gate	8020086	————
U5	74121, Monostable multivibrator single, not retriggerable	8000121	————
U6	74LS164, 8-bit parallel-out serial shift register	8020164	————
U7	74LS244, Line driver	8020244	AMX3864
U8	74LS273, Octal "D" flip-flop	8020273	AMX4227
U9	2316E, Mask ROM, 450ns access	8043316	————
U10	74LS165, Parallel-load 8-bit shift register	8020165	————
U11	6845, CRT controller	8050845	AXX3019
U12	74LS174, Dual "D" flip-flop	8020174	AXX3565
U13	74LS08, Quad, 2-input AND gate	8020008	————

VIDEO/KEYBOARD INTERFACE BOARD PARTS LIST (Cont'd)

SYMBOL	DESCRIPTION	MANUFACTURER'S PART NUMBER	RADIO SHACK PART NUMBER
	INTEGRATED CIRCUITS (Cont'd)		
U14	74LS33, Quad 2-input NOR buffer	8020033	————
U15	74LS11, Triple 3-input AND gate	8020011	AMX3554
U16	74LS74, Dual "D" flip-flop positive-edge-triggered	8020074	AMX3558
U17	74LS74, Dual "D" flip-flop positive-edge-triggered	8020074	AMX3558
U18	74LS175, Quad "D" flip-flop	8020175	AMX3566
U19	2114, RAM, 1024-by-4 bit	8040004	————
U20	2114, RAM, 1024-by-4 bit	8040004	————
U21	2114, RAM, 1024-by-4 bit	8040004	————
U22	2144, RAM, 1024-by-4 bit	8040004	————
U23	74LS157, Quad 2-to-1 line selector/multiplexer	8020157	AMX3563
U24	74LS157, Quad 2-to-1 line selector/multiplexer	8020157	AMX3563
U25	74LS157, Quad 2-to-1 line selector/multiplexer	8020157	AMX3563
U26	74LS161, Synchronous 4-bit counter	8020161	————
U27	74LS30, 8-input NAND gate	8020030	AMX3556
U28	74LS00, Quad 2-input NAND gate	8020000	AMX3550
U29	74LS08, Quad, 2-input AND gate	8020008	————
U30	74LS04, Hex inverter	8020004	AMX3552
U31	74LS155, Dual 2-to-4 line decoder/demultiplexer	8020155	————
U32	74LS76, Dual J-K flip-flop with preset and clear	8020076	————
U33	74LS04, Hex inverter	8020004	AMX3552
U34	8T26A, Bus transceiver	8060026	AMX4261
U35	8T26A, Bus transceiver	8060026	AMX4261
U36	8T26A, Bus transceiver	8060026	AMX4261
U37	8T26A, Bus transceiver	8060026	AMX4261
U38	74LS240, Octal buffer	8020240	AMX4225
U39	74LS240, Octal buffer	8020240	AMX4225
U40	74LS240, Octal buffer	8020240	AMX4225
U41	74LS30, 8-input NAND gate	8020030	AMX3556
U42	74LS00, Quad 2-input NAND gate	8020000	AMX3550
	MISCELLANEOUS		
	Plug, jumper (2)	8519021	AJ6769
	Socket, IC, 40-pin	8509002	AJ6580
	Socket, IC, 24-pin	8509001	AJ6579
	Socket, IC, 18-pin (4)	8509006	AJ6701
	Stake pin (24)	8529014	AHB9682

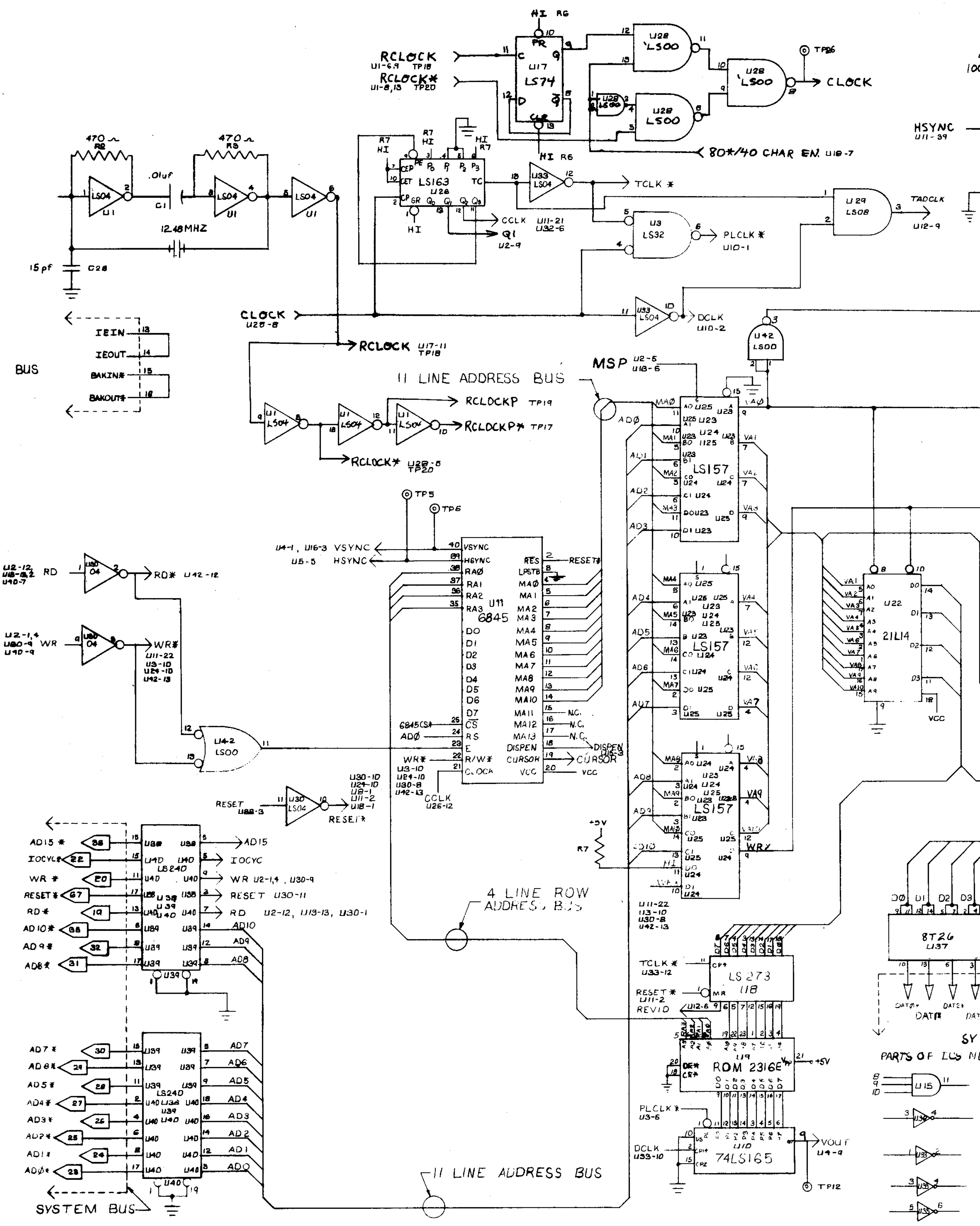
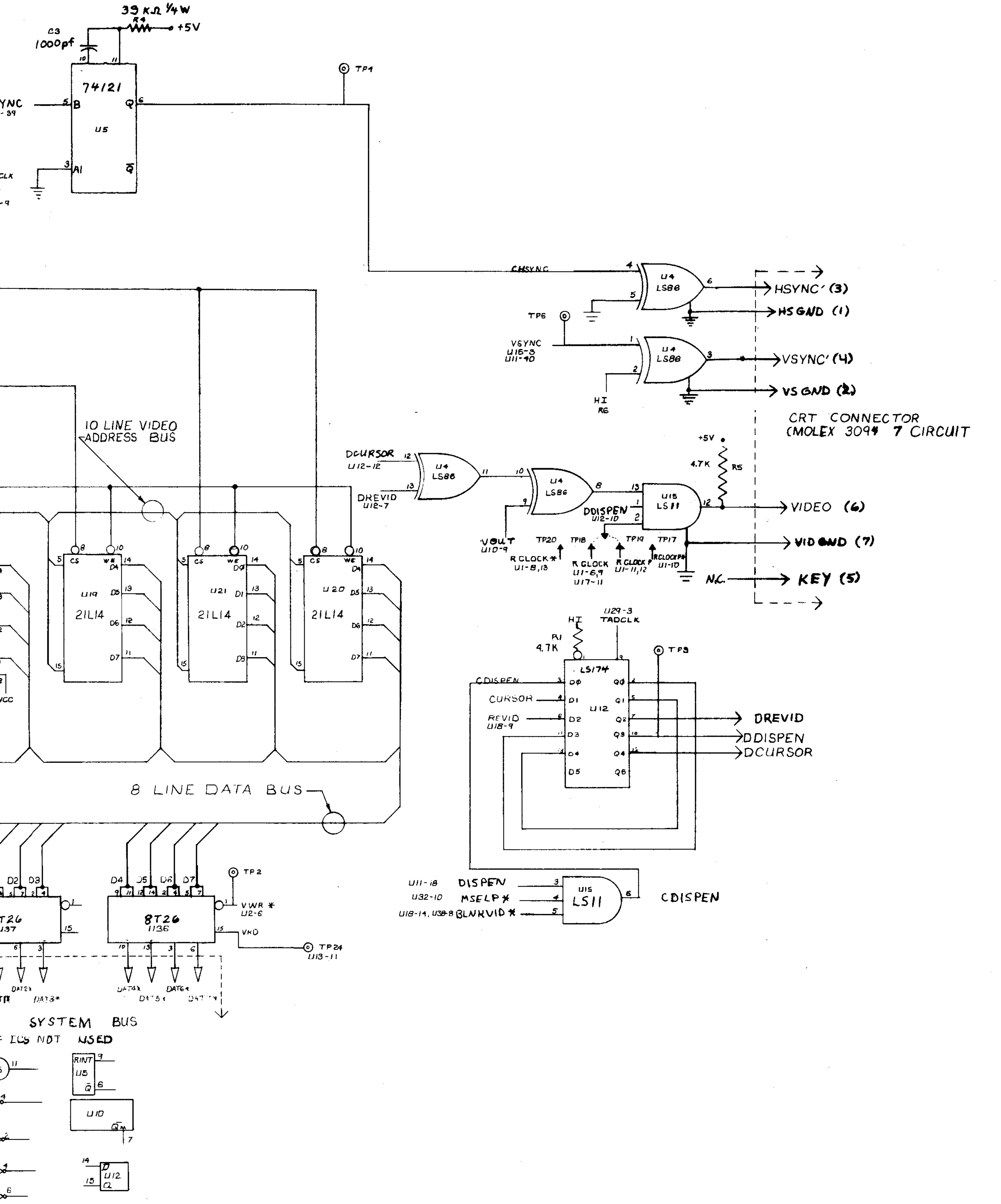


Figure 8. Video/Keyboard Interfa



Interface Schematic Diagram (Sheet 1)

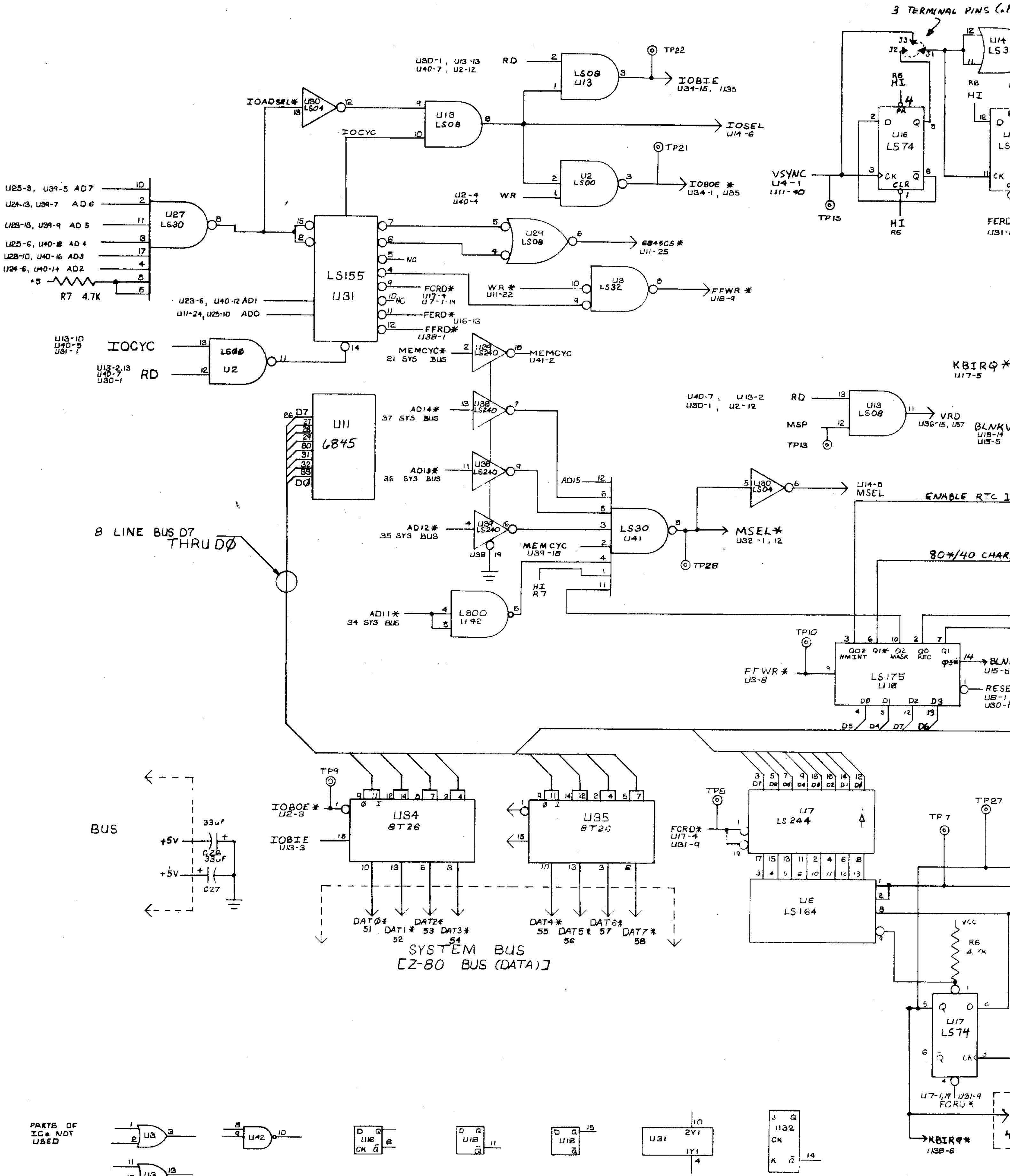
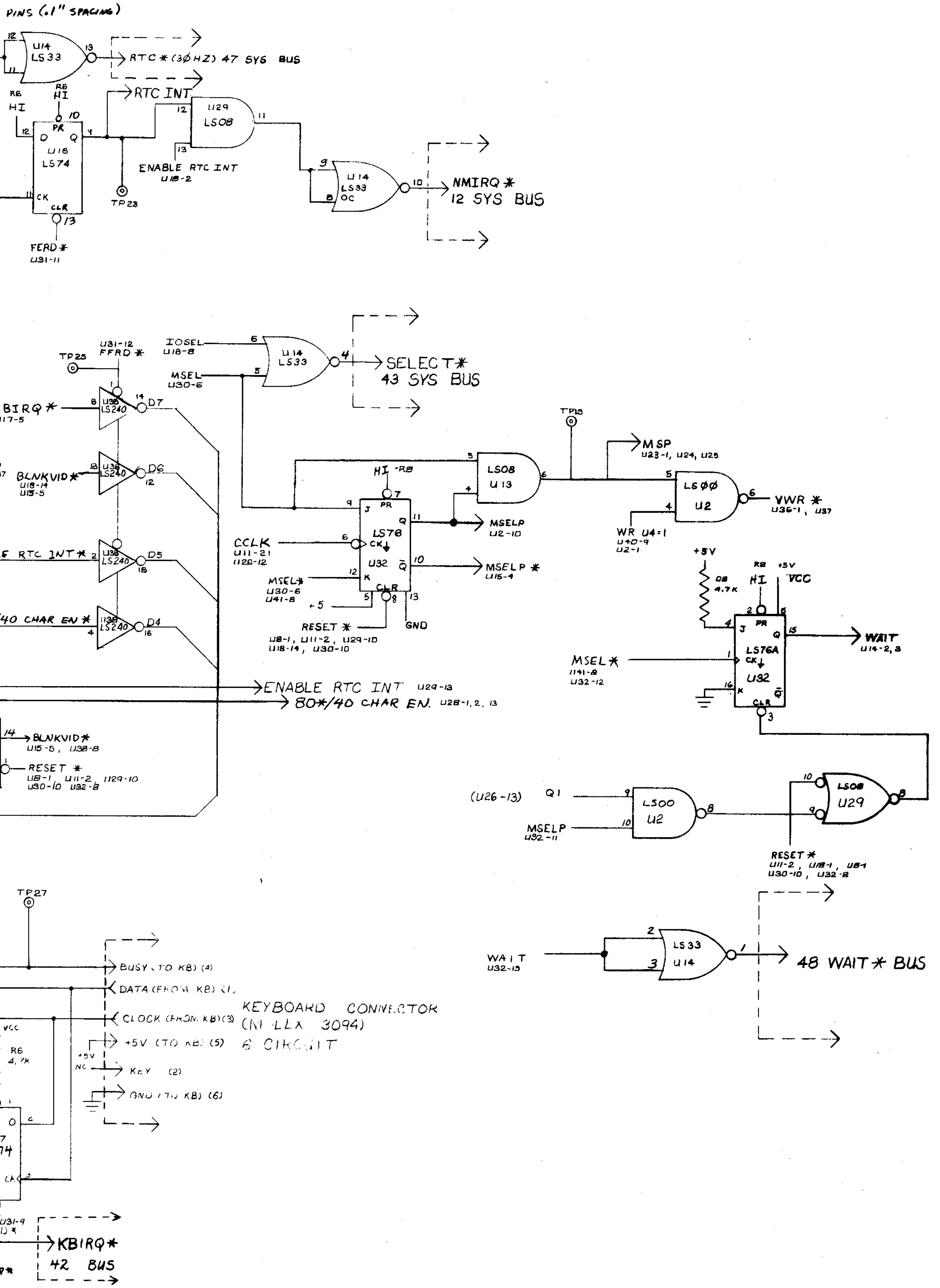


Figure 8. Video/Keyboard Interface Sch



face Schematic Diagram (Sheet 2)

SECTION VI

MEMORY BOARD (64K and 32K RAM)

A. FUNCTIONAL SPECIFICATIONS

1. **Interface** – The interface between the memory board and the Model II bus is fully buffered. Any line used by the memory board presents only one unit load on that particular line. (One unit load being the load presented by an LS-TTL device.)
2. **Memory array** – The memory array uses 16K dynamic memory chips. The board comes with either 32K bytes of RAM or 64K bytes of RAM.
3. **Timing** – The generation of MUX and CAS for the memory array is accomplished by the use of a delay line which allows precise memory timing.
4. **Paging** – The memory is logically divided into 32K byte pages. Page zero consists of all memory from ØØØØ to 7FFF Hexadecimal addresses and pages 1 to 15 consist of all memory from 8ØØØ Hex to FFFF Hex. Only one of the memory pages 1 to 15 is enabled at one time. The state of the lower four bits of Port FF determines which one of these pages is enabled.
5. **Bank Select** – Each memory board has the option of being selected as one of eight banks by using the bank select option in conjunction with the bank select bits in Port FF. Each bank contains two 32K byte pages. Therefore it is theoretically possible to have 512K bytes of random access memory in a system.

B. THEORY OF OPERATION

Refer to Memory Board Schematic

1. **Interface** – The interface to the Model II system bus consists of:
   A) Data Bus Buffers
   B) Address Buffers
   C) Control Line Buffers
   The data bus buffer-drivers buffer input data from the CPU and output data to the CPU. They consist of chips U53 and U52. Gating logic is performed by U26, U14, U27 and U12.

   The address buffers buffer and invert the address signals and present them to the multiplexers (U39 and U40), to the port select logic (U41) and to the memory select logic (U10, U11, U14 and U29).

   The control line buffers provide the following signals to the memory board – SYNC*, CLOCK, MEMCYC*, RD*, REFRSH*, WR*, IOCYC* and RESET* which are used by the RAS precharge extender circuit (U14, U18). This insures that the minimum precharge time will be provided by the 4MHz CPU to the memory chips. RD* is used by U27 to gate data onto the bus. REFRSH* is used by U14 and U24 in generating the memory refresh pulse; WR* is buffered directly into the memory array and to U41 for the I/O port write pulse. IOCYC* is also used by U41 for the same purpose. RESET* is used to clear port FF.

2. **Memory Array** – The memory array consists of 16 or 32 chips. The chips are 16K by 1 bit MOS dynamic memory circuits. Thus, one will have either a 32K byte memory board or a 64K byte memory board. All the power supply voltages are bypassed on every other chip to provide good noise immunity. The RAM chips are U1 – U8, U15 – U22, U30 – U37 and U44 – U51. 12 volt bulk capacitance is provided on the memory array since this is the supply voltage most heavily used. These are – C13, C25, C39 and C57.

3. **Address Multiplexers** – The address multiplexers U39 and U40 take the buffered address and drive the memory array through damping resistors U38 (dip resistor array). The MUX signal provided by the timing section switches between the row address and the column address. The damping resistors minimize the undershoot on the signal lines which further enhances error free operation.

4. **Timing** – The timing consists of circuits U13, U14 (precharge extender), U42 (delay line), U57 (delay line buffer), U28 (CAS and MUX buffers) and U9 (CAS and write drivers). When MEMCYC* is active, indicating that the CPU is going to do a read or a write, RAS is generated by the precharge circuitry and is gated with REFRSH* at U14 (i.e., no RAS pulse is passed to the delay line during Refresh). The resulting pulse propagates down the delay line; generating first, MUX which switches the address multiplexers from Row address to Column address, and second, it generates CAS which provides (through drivers) the signal of the same name to the memory array.

   RAS is also buffered by U24 to provide RAS to the memory array. If WR* was present on the bus then it is appropriately buffered into the memory array and signals a write cycle; otherwise, the data from the memory array is available for a read cycle. Note also that all RAS, CAS, and WR signals are damped into the memory array just as the address lines are and for the same reason. The damping resistor package is U23.

5. **Memory select logic** – The memory select logic consists of packages U29, U43 and U24. The buffered address lines A14 and A15 and bits Ø to 3 of Port FF are combined to produce select signals for pages 1 to 15. The memory select signal is then OR'd with Refresh and the resulting signal gates RAS into the memory array through NAND gates U24.

6. **Memory disable logic** – This logic is used to disable memory from F8ØØ to FFFF when one wishes to access video memory that is mapped into the same physical address space. Only memory pages 1 to 15 are affected. Circuit U11 decodes the memory address range, the memory page being accessed, and the video RAM enable bit (bit 7) from I/O port FF. It also produces the gate signal for 74S139 decoder controlling

the memory select signals for pages 1 to 15. If the gate signal is not present (pin 1 of the 74S139) then no memory access is allowed.

7. **I/O Port FF and Select logic** – I/O port FF is package U58 which is an 8-bit register and is selected by the strobe $\overline{\text{IOFFWR}}$ which is generated by U41. U41 decodes the lower 8 address lines, IOCYC and the WR line to generate the select. The RESET line clears Port FF on power-up or manual reset. The lower four bits of this register drive the Bank select logic which selects one of memory pages 1 to 15. Bit 7 of this register is the Video RAM enable bit which feeds the Memory disable logic.

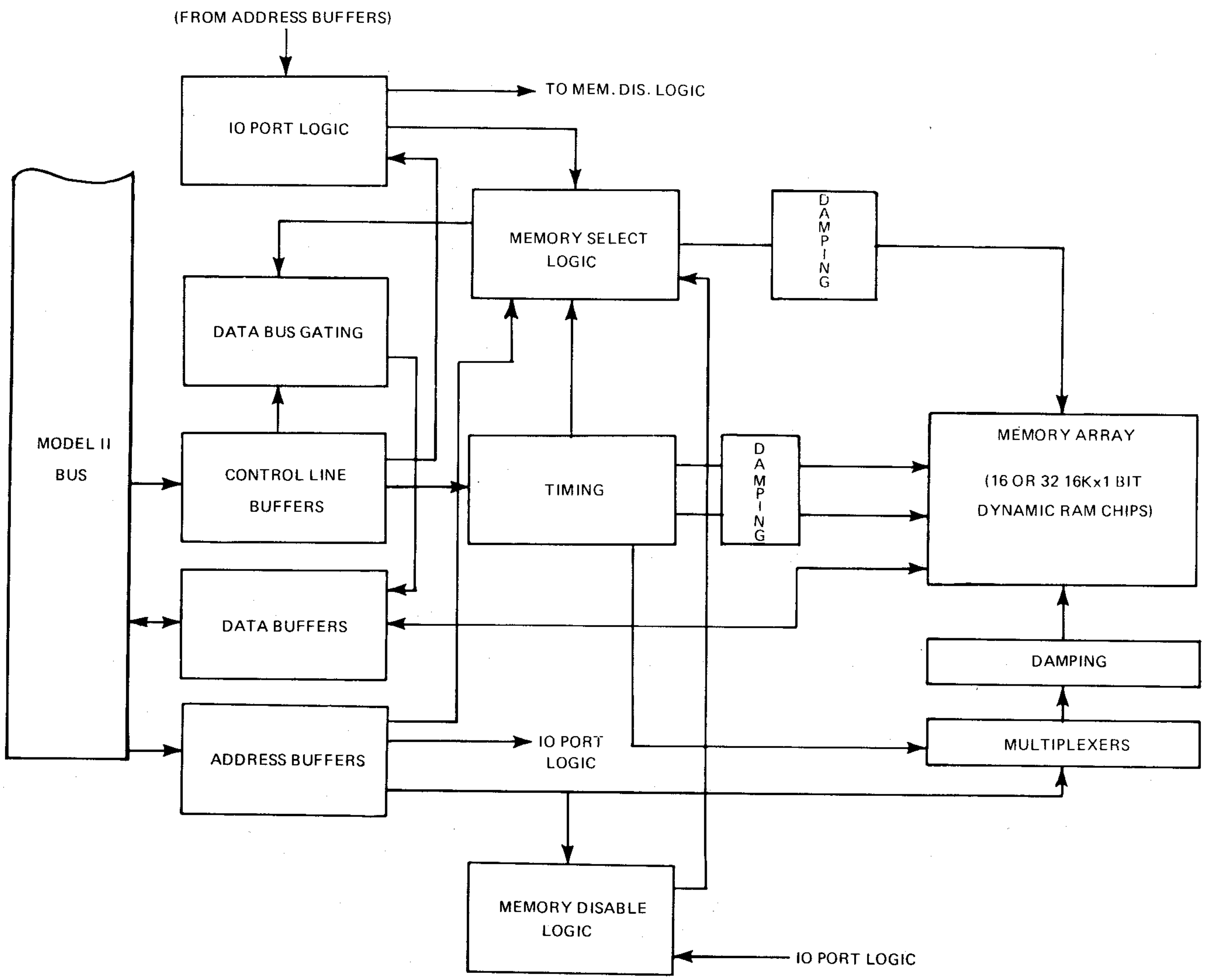


Figure 1. Block Diagram

C. JUMPER OPTIONS

The following table lists all the jumper options. Also refer to Figure 2.

Memory Page	Memory Bank	Memory Page Jumpers	Memory Bank Jumpers
0	0	J16-J17, J15-J18	
1	0	J9-J13, J10-J14	J19-J27
1*	0	J9-J11, J10-J12	J19-J27
2	1	J7-J11, J8-J12	J20-J28
3	1	J9-J13, J10-J14	J20-J28
4	2	J7-J11, J8-J12	J21-J29
5	2	J9-J13, J10-J14	J21-J29
6	3	J7-J11, J8-J12	J22-J30
7	3	J9-J13, J10-J14	J22-J30
8	4	J7-J11, J8-J12	J23-J27
9	4	J9-J13, J10-J14	J23-J27
10	5	J7-J11, J8-J12	J24-J28
11	5	J9-J13, J10-J14	J24-J28
12	6	J7-J11, J8-J12	J25-J29
13	6	J9-J13, J10-J14	J25-J29
14	7	J7-J11, J8-J12	J26-J30
15	7	J9-J13, J10-J14	J26-J30

*Jumper configuration for add-on 32K memory board.

For example: A 32K memory board will have Page Ø and jumpers as above. The first 64K memory board will have Page Ø and Page 1 and jumpers as above.

D. VERIFICATION PROCEDURES

1. Automatic RAM verification is performed on the memories during the boot procedures. If an error is encountered, an MF error is displayed in the center of the CRT screen.

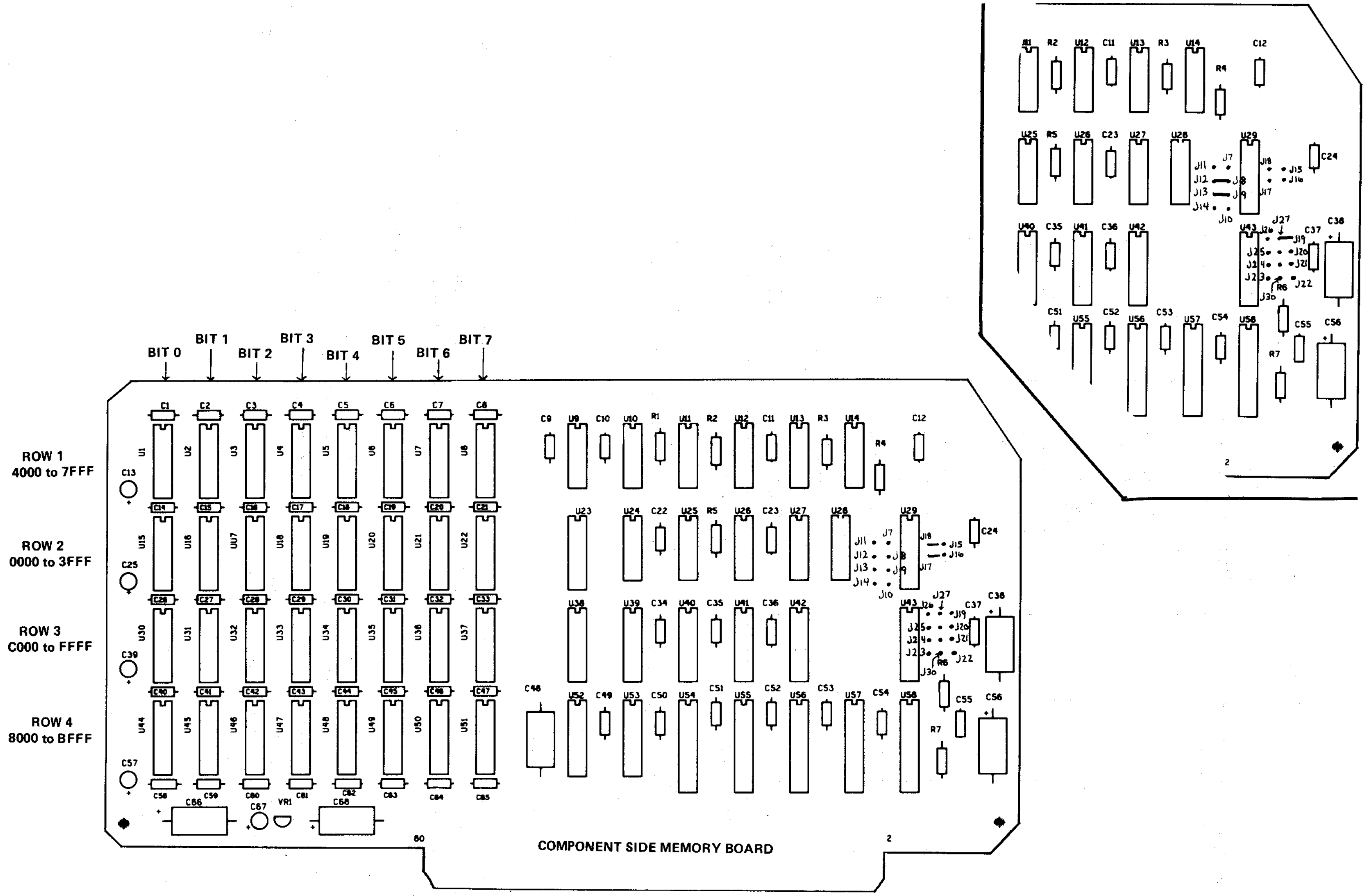
IMPORTANT NOTE

The test procedures below should *never* be attempted by an unqualified technician. If the diagnostic instructions are not followed correctly the computer video can and probably will be damaged. We strongly suggest that if these procedures are necessary, you should return your unit to Radio Shack.

2. Further testing can be done on the system memories by using the Diagnostic Diskette and the TRS-80 Model II Troubleshooting Manual.

WARNING

When performing a test that includes turning the CRT on and off, *do not* leave it off for more than three seconds or damage to the circuitry may occur.



Note: Inset shows jumper configuration for standard 64K board.

Figure 2. Jumper Locations for Standard 32K Board and Address/Bit RAM Identification.

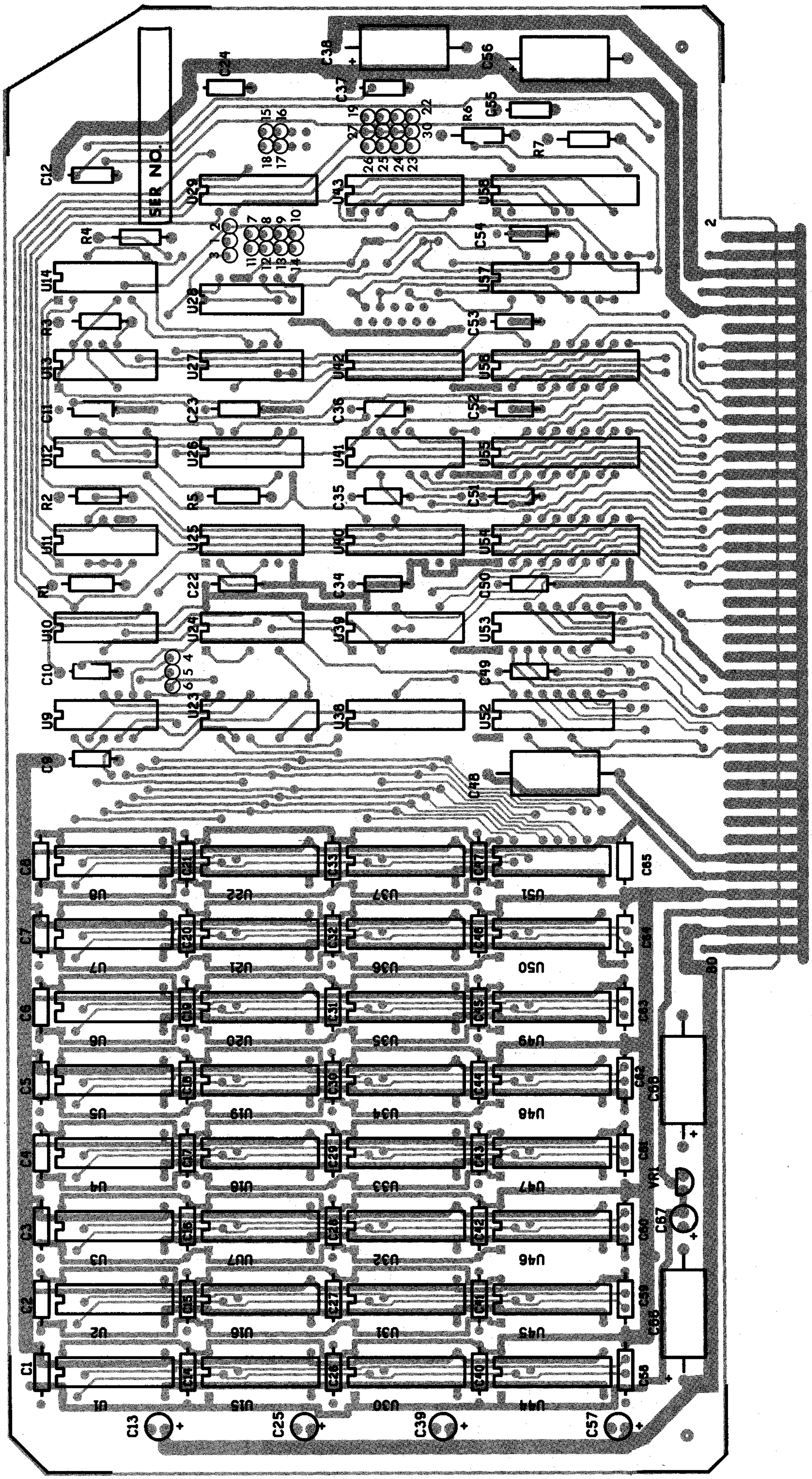


Figure 3. 32K and 64K RAM Memory Board Printed Circuit Board — Component Side

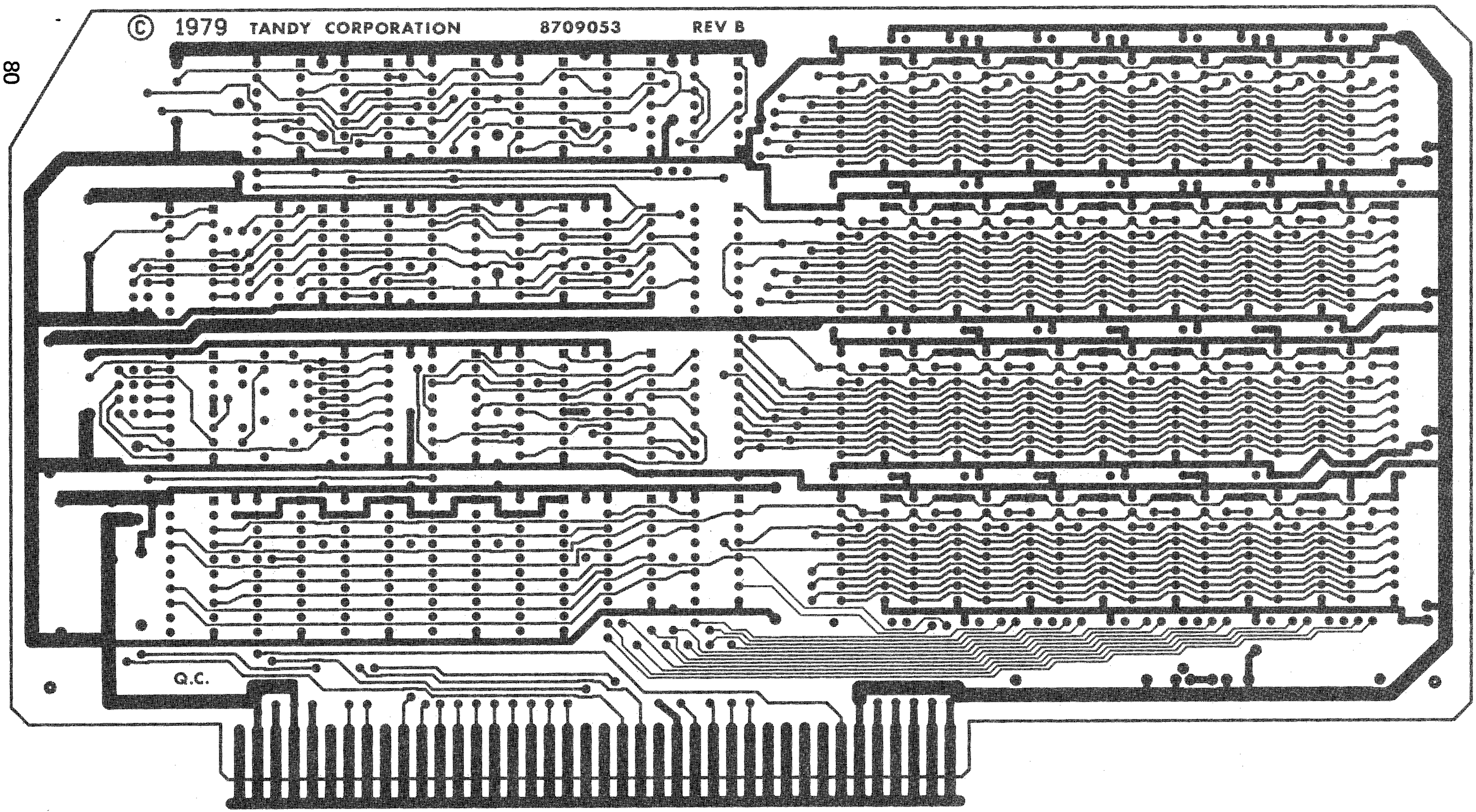


Figure 4. 32K and 64K RAM Memory Board Printed Circuit Board — Circuit Side

MEMORY BOARD (32K & 64K) PARTS LIST

SYMBOL	DESCRIPTION	MANUFACTURER'S PART NUMBER	RADIO SHACK PART NUMBER
	ELECTRICAL		
	PC Board	8709053	—
	CAPACITORS		
C1	0.1μF, 50V, Monolithic	8374104	—
↓	↓ ↓	↓	↓
C12	0.1μF, 50V, Monolithic	8374104	—
C13	4.7μF, 25V, Electrolytic, PC	8325472	ACC475QFA
C14	0.1μF, 50V, Monolithic	8374104	—
↓	↓ ↓	↓	↓
C24	0.1μF, 50V, Monolithic	8374104	—
C25	4.7μF, 25V, Electrolytic	8325472	ACC475QFA
C26	0.1μF, 50V, Monolithic	8374104	—
↓	↓ ↓	↓	↓
C37	0.1μF, 50V, Monolithic	8374104	—
C38	33μF, 25V, Electrolytic, Axial	8316332	—
C39	4.7μF, 25V, Electrolytic, PC	8325472	ACC475QFA
C40	0.1μF, 50V, Monolithic	8374104	—
↓	↓ ↓	↓	↓
C47	0.1μF, 50V, Monolithic	8374104	—
C48	33μF, 25V, Electrolytic	8316332	—
C49	0.1μF, 50V, Monolithic	8374104	—
↓	↓ ↓	↓	↓
C55	0.1μF, 50V, Monolithic	8374104	—
C56	33μF, 25V, Electrolytic	8316332	—
C57	4.7μF, 25V, Electrolytic	8325472	ACC475QFA
C58	0.1μF, 50V, Monolithic	8374104	—
↓	↓ ↓	↓	↓
C65	0.1μF, 50V, Monolithic	8374104	—
C66	33μF, 25V, Electrolytic	8316332	—
C67	10μF, 16V, Electrolytic, PC	8326101	—
C68	33μF, 25V, Electrolytic, Axial	8316332	—
*C69	0.1μF, 50V, Monolithic	8374104	—
	RESISTORS		
R1	4.7K, 1/4W, 5%, Carbon Film	8207247	AN0247EEC
R2	1K, 1/4W,, 5%, Carbon Film	8207210	AN0196EEC
R3	4.7K, 1/4W, 5%, Carbon Film	8207247	AN0247EEC
R4	4.7K, 1/4W, 5%, Carbon Film	8207247	AN0247EEC
R5	4.7K, 1/4W, 5%, Carbon Film	8207247	AN0247EEC
R6	100 ohm, 1/4W, 5%, Carbon Film	8207110	AN0132EEC
R7	4.7K, 1/4W, 5%, Carbon Film	8207247	AN0247EEC
*R8	220 ohm, 1/2W, 5%, Carbon Film	8217122	AN0149EEC

*May appear on your Board in combination with zener diode, Part Number 8150230.

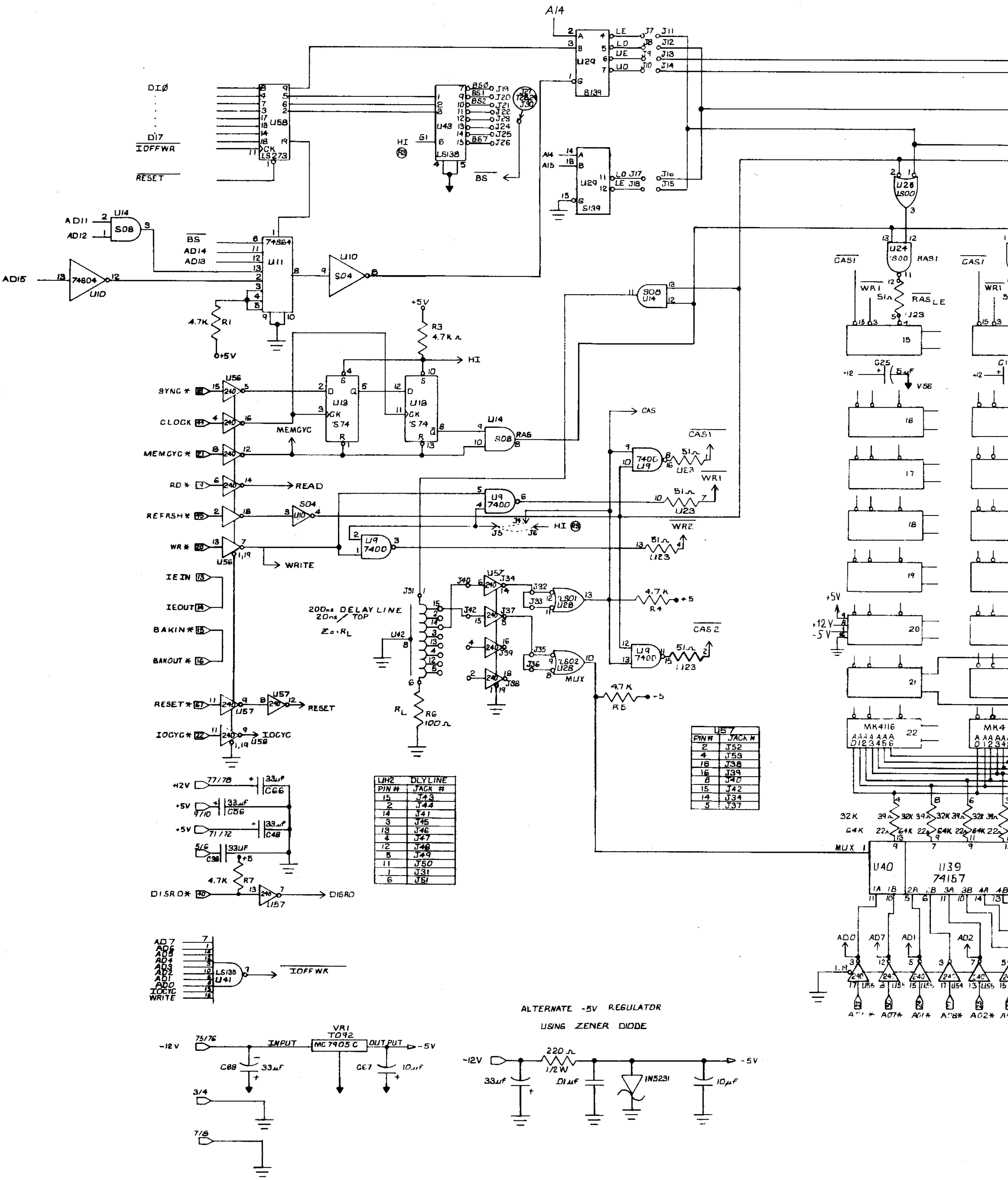
MEMORY BOARD (32K & 64K) PARTS LIST (Cont'd)

SYMBOL	DESCRIPTION	MANUFACTURER'S PART NUMBER	RADIO SHACK PART NUMBER
	INTEGRATED CIRCUITS		
U1	MK4116-3, 16K RAM	9040016	AXX3024
↓	↓ ↓	↓	↓
U8	MK4116-3, 16K RAM	9040016	AXX3024
U9	7400, Quad 2-input NAND gate	8000000	————
U10	74S04, Hex inverter	8010004	————
U11	74S64, 4-2-3-2 input AND-OR inverter with totem pole output	8010064	————
U12	74LS33, Quad 2-input NOR buffer with open collector outputs	8020033	————
U13	74S74, Dual "D" flip-flop positive-edge-triggered	8010074	AMX3558
U14	74S08, Quad 2-input AND gate	8010008	————
U15	MK4116-3, 16K RAM	9040016	AXX3024
↓	↓ ↓	↓	↓
U22	MK4116-3, 16K, RAM	9040016	AXX3024
U23	47 ohm DIP resistor pak, 16-pin	8290004	ARX0169
U24	74S00, Quad 2-input NAND gate	8010000	————
U25	74LS00, Quad 2-input NAND gate	8020000	AMX3550
U26	74LS20, Dual 4-input NAND gate	8020020	AMX3555
U27	74LS10, Triple 3-input AND gate	8020010	————
U28	74LS02, Quad 2-input NOR gate	8020002	AMX3551
U29	74S139, Dual 2-to-4 line decoder/multiplexer	8010139	————
*U30	MK4116-3, 16K RAM	9040016	AXX3024
↓	↓ ↓	↓	↓
*U37	MK4116-3, 16K, RAM	9040016	AXX3024
U38	39 ohm DIP resistor pak 16-pin	8290002	ARX0167
*U38	22 ohm DIP resistor pak 16-pin	8290005	ARX0170
U39	74157, Quad 2-to-1 line data selector/multiplexer with non-inverted data outputs	8000157	————
U40	74157, Quad 2-to-1 line data selector/multiplexer with non-inverted data outputs	8000157	————
U41	74LS133, 13-input NAND gate	8020133	AMX3927
U42	200ns DIP delay line	8429004	AMX4264
U43	74LS138, 3-to-8 line decoder/multiplexer	8020138	
*U44	MK4116-3, 16K RAM	9040016	AMX3024
↓	↓ ↓	↓	↓
*U51	MK4116-3, 16K RAM	9040016	AMX3024
U52	8T26A, Bus transceiver	8060026	AMX4261
U53	8T26A, Bus transceiver	8060026	AMX4261
U54	74LS240, Octal buffer	8020240	AMX4225
U55	74LS240, Octal buffer	8020240	AMX4225
U56	74LS240, Octal buffer	8020240	AMX4225
U57	74LS240, Octal buffer	8020240	AMX4225
U58	74LS273, Octal "D" flip-flop common clock single rail output	8020273	AMX4227

MEMORY BOARD (32K & 64K) PARTS LIST (Cont'd)

SYMBOL	DESCRIPTION	MANUFACTURER'S PART NUMBER	RADIO SHACK PART NUMBER
	VOLTAGE REGULATOR		
†VR1	MC79L05AC, - 5V, 5%, TO-92 case	8051905	AMX4260
†May also appear as:			
VR1	1N5231, Zener diode	8150230	ADX1211
	MISCELLANEOUS		
	Plug, Jumper (5)	8519021	AJ6769
	Socket, IC, 16-pin (16)	8509003	AJ6581
	*Socket, IC, 16-pin (32)	8509003	AJ6581
	Stake Pin (52)	8529014	AHB9682

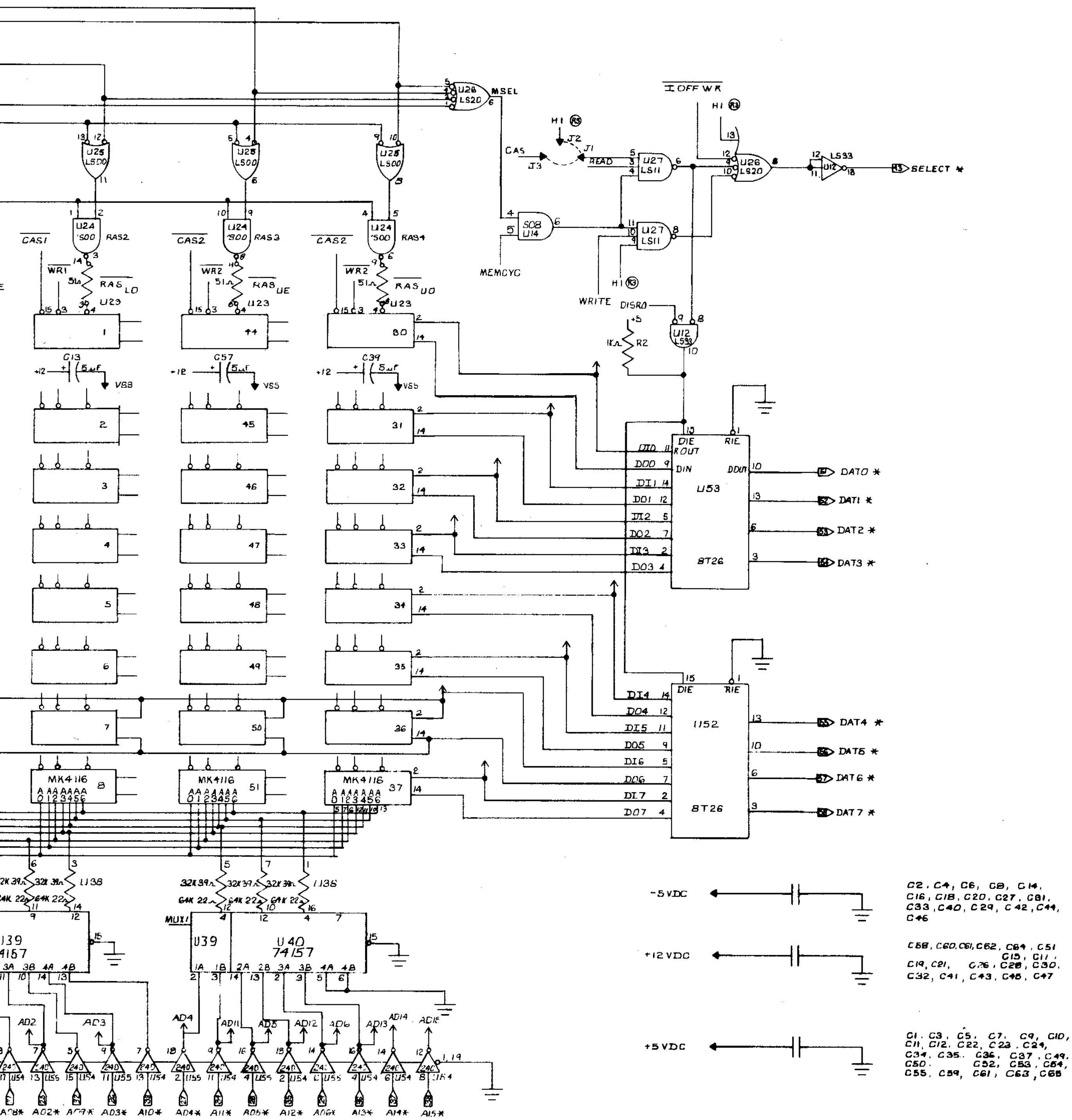
*Used only on the 64K RAM Memory Board.



U42	DLYLINE
PIN #	JACK #
15	J43
2	J44
14	J41
3	J45
13	J46
4	J47
12	J48
5	J49
11	J50
1	J31
6	J51

U57	
PIN #	JACK #
2	J52
4	J53
18	J38
16	J39
8	J40
15	J42
14	J34
5	J37

Figure 5. Memory Boa



emory Board Schematic Diagram

SECTION VII

VIDEO MONITOR (CRT)

VIDEO MONITOR
(MOTOROLA)

A. FUNCTIONAL SPECIFICATIONS

General Information

All models are direct drive, requiring separate TTL vertical/horizontal drive and video inputs. All use 12" CRTs of the magnetic deflection type with integral implosion protection and require a power input of +12 volts@ 1.2 amps.

Input and output connections for the monitor are made through a 10-pin circuit card edge connector. The inputs are video, horizontal drive, vertical drive, system ground, and +12 volts.

A single circuit card with components mounted on one side is used. Schematic reference numbers are printed on both sides of the circuit card to aid in the location and identification of components for servicing.

Circuitry consists of one stage of video amplification, two stages of horizontal deflection processing, and three stages of vertical deflection processing.

SPECIFICATIONS

ITEM	SPECIFICATION
Cathode Ray Tube:	12" measured diagonally (305 mm); 74.86 square inches (483 sq. cm); 90° deflection angle; integral implosion protection, P4 phosphor standard.
Power Input:	+12 VDC at 1.2 amps typical, 1.5 amps maximum.
TTL Level Direct Drive Input Signals:	1.5 to 5V P-P Horizontal: 10 to 30 microseconds positive-going drive, Vertical: negative-going sync, Video: positive white
Video Response:	Bandwidth within 3dB, 10Hz to 15MHz typical.
Pulse Rise Time:	30V rise in less than 30 nanoseconds.
Horizontal Blanking Interval:	11 microseconds minimum (includes retrace and delay).
High Voltage:	12kV typical.
Scanning Frequency:	Horizontal: 15,750Hz ± 500Hz; Vertical: 50/60Hz.
Resolution:	800 lines center, typical.
Geometric Distortion:	within 2% measured with standard EIA ball chart and dot pattern.
Linearity:	within 10% measured with standard EIA ball chart and dot pattern.
Controls:	Internal — horizontal size, vertical size, vertical linearity, internal brightness. External — brightness control, video level (contrast).
Unit Weight:	8½ lbs. (3.86 kg).
Environment:	Operating temperature: 32°F to 131°F (0°C to +55°C). Storage temperature: −40°F to 150°F (−40°C to +65°C). **NOTE:** Models with bonded anti-reflective faceplates should not be subjected to storage or operating temperatures above 122°F (50°C). Operating altitude: 10,000 ft. maximum (3046 meters).

SAFETY WARNING

CAUTION: NO WORK SHOULD BE ATTEMPTED ON AN EXPOSED MONITOR CHASSIS BY ANYONE NOT FAMILIAR WITH SERVICING PROCEDURES AND PRECAUTIONS.

1. SAFETY PROCEDURES should be developed by habit so that when the technician is rushed with repair work, he automatically takes precautions.

2. A GOOD PRACTICE, when working on any unit, is to first ground the chassis and to use only one hand when testing circuitry. This will avoid the possibility of carelessly putting one hand on chassis or ground and the other on an electrical connection which could cause a severe electrical shock.

3. Extreme care should be used in HANDLING THE PICTURE TUBE as rough handling may cause it to implode due to atmospheric pressure (14.7 lbs. per sq. in.). Do not nick or scratch glass or subject it to any undue pressure in removal or installation. When handling, safety goggles and heavy gloves should be worn for protection. Discharge picture tube by shorting the anode connection to chassis ground (not cabinet or other mounting parts). When discharging, go from ground to anode or use a well insulated piece of wire.

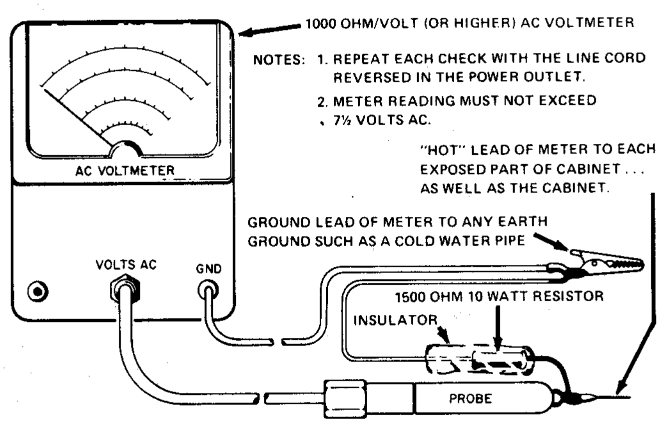
4. An ISOLATION TRANSFORMER should always be used during the servicing of a unit whose chassis is connected to one side of the power line. Use a transformer of adequate power rating as this protects the serviceman from accidents resulting in personal injury from electrical shocks. It will also protect the chassis and its components from being damaged by accidental shorts of the circuitry that may be inadvertently introduced during the service operation.

5. Always REPLACE PROTECTIVE DEVICES, such as fishpaper, isolation resistors and capacitors and shields after working on the unit.

6. If the HIGH VOLTAGE is adjustable, it should always be ADJUSTED to the level recommended by the manufacturer. If the voltage is increased above the normal setting, exposure to unnecessary X-ray radiation could result. High voltage can accurately be measured with a high voltage meter connected from the anode lead to chassis.

7. BEFORE RETURNING A SERVICED UNIT, the service technician must thoroughly test the unit to be certain that it is completely safe to operate without danger of electrical shock. DO NOT USE A LINE ISOLATION TRANSFORMER WHEN MAKING THIS TEST.

In addition to practicing the basic and fundamental electrical safety rules, the following test, which is related to the minimum safety requirements of the Underwriters Laboratories should be performed by the service technician before any unit which has been serviced is returned.



Voltmeter Hook-up for Safety Check

A 1000 ohm per volt AC voltmeter is prepared by shunting it with a 1500 ohm, 10 watt resistor. The safety test is made by contacting one meter probe to any portion of the unit exposed to the operator such as the cabinet trim, hardware, controls, knobs, etc., while the other probe is held in contact with a good "earth" ground such as a cold water pipe.

The AC voltage indicated by the meter may not exceed 7½ volts. A reading exceeding 7½ volts indicates that a potentially dangerous leakage path exists between the exposed portion of the unit and "earth" ground. Such a unit represents a potentially serious shock hazard to the operator.

The above test should be repeated with the power plug reversed, when applicable.

NEVER RETURN A MONITOR which does not pass the safety test until the fault has been located and corrected.

B. SERVICE NOTES

1. **Circuit Tracing:**

   Component reference numbers are printed on the top and bottom of the three circuit cards to facilitate circuit tracing. Control names are also shown and referenced on the schematic diagram.

2. **CRT Replacement:**

   Replace the CRT as described in section F. Additional precautions to be observed are as follows:

   Use extreme care in handling the CRT, as rough handling may cause it to implode, due to high vacuum pressure. Do not nick or scratch glass or subject it to any undue pressure in removal or installation. Use goggles and heavy gloves for protection. Also, be sure to disconnect the monitor from all external voltage sources.

   Use caution around the heat sinks of the horizontal and vertical output transistors. The heat sinks are at the same potential as the transistor collectors. During normal operation with a signal input present, the horizontal heat sink has 130 volt P-P pulses and the vertical heat sink has 75 volt P-P pulses (with respect to system ground).

3. Before working on the Video/Model II, observe these precautions:

   a. Remove all jewelry.

   b. Discharge the two large grey high-voltage capacitors (on the Astec Power Supply) across their own terminals with an insulated screw driver.

   NOTE

   Be sure to ground the discharging tool with a clip wire to ground before attempting to discharge the capacitors.

   c. On the Motorola Video Board, discharge capacitor C6 and **very carefully** discharge to ground the thick, red to black high-voltage second anode lead.

   WARNING

   This lead (black) plugs into a sleeving that goes to the CRT Driver Board while the other lead (red) connects to the CRT shell. Discharge by unplugging the lead from the sleeving near the Driver Board and shorting the lead to chassis ground. **Do not touch the conductor of this lead! 12000 volts reside here!**

   d. The CRT socket, deflection yoke and the second anode lead can now be safely removed.

Of course, these precautions, with the exception of step b, only apply if the machine is to be serviced with power off. If active test instrument troubleshooting is to be done and power must be on, be very aware of where your hands are and remain alert. High voltages can harm you and even low voltages can harm circuits when unintentional shorting of wires and subassemblies occurs.

C. ADJUSTMENTS

1. **Brightness/Contrast Adjustment**

   A non-metallic tool is recommended when performing the following adjustments.

   a. Rotate the Contrast control to minimum.

   b. Rotate the Internal Brightness control, R11, to minimum (fully clockwise).

   c. Rotate the External Brightness control to its maximum position.

   d. Rotate R11 to the threshold of the raster.

   e. Adjust the Contrast control for the desired video level.

   f. Adjust the External Brightness control for the desired brightness level.

   g. The following adjustments will require the use of the Diagnostic Diskette and the Troubleshooting Manual:

   Vertical Size/Linearity Adjustment

   Focus Adjustment

   Horizontal Size Adjustment

   Video Centering

   Raster Yoke Adjustments

   Pincushion/Barrel Correction

   Trapezoidal Correction.

D. TROUBLESHOOTING GUIDE

A. There are basically six areas that may cause the loss, distortion or non-adjustment of video. These areas are:

1. System Power Supply
2. Video Generator Module
3. Motorola Video Board
4. Cathode Ray Tube
5. CRT Deflection Coil
6. High voltage leads from the CRT

(Don't overlook any of the interconnecting wiring between these assemblies.)

B. Listed below are some of the symptoms and their possibles causes and remedies:

SYMPTOM	POSSIBLE CAUSE	REMEDY
No video at all	Video Generator Module or Motorola Video Board or Power Supply or any combination of the above	Check voltage from Power Supply at pin 7 of the plug connecting at the top of the Motorola Video Board. **NOTE**: Pin 1 is to the back of the system. Voltage should be approximately 12 VDC. No voltage indicates a bad Power Supply. Check pin 6 of the same plug for a 2 volt peak-to-peak signal[1] of approximately 15,750 Hz. If no signal is there, replace the Video Generator Module[2]. Check pin 8 of the same plug for approximately 1.5 volts peak-to-peak signal[1]. If no signal is present, replace the Video Generator Module.
Thin horizontal or vertical line on video screen; no video elsewhere on screen	Deflection coil	Replace Deflection Yoke.
Thin horizontal line	Q7 on Motorola Video Board	Replace Q7 and, with power off and green and blue wires disconnected, check continuity across deflection coil where green and blue wires are hooked up. An open, or high resistance, indicates a defective deflector coil.
Thin vertical line	Q4 on Motorola Video Board	Replace Q4 and, with power off and red and black wires disconnected, check continuity between the points that the red and black wires are connected to. An open, or high resistance, indicates a defective deflector coil.
Video is off center on screen	Video Centering magnets on deflection coil need to be adjusted	Adjust Video Centering Magnets for best centering of video on screen (remove all jewelry and use caution, **remember, the system is on!**).
Bad focus	R30 of the Motorola Video Board needs to be adjusted	Adjust R30 as necessary for sharpest focus. **NOTE**: Be careful not to short the adjustment tool to other components.

SYSTEM	POSSIBLE CAUSE	REMEDY
Insufficient brightness	R11 of the Motorola Video Board needs adjusting	Adjust brightness on front bezel of the computer to mid-travel then adjust R11 of Motorola Video Board to desired screen brightness.
No Sync on screen[3] no horizontal or vertical hold	Video Generator Module (VGM)	Replace U11 (Video Controller[4]). If the problem is not corrected, replace VGM.
Jittering of video and intermittent dropping out and reappearing of video dots on the screen	High voltage leak or leaks	With power off and capacitors discharged, check high-voltage leads for breaks, kinks or placed too close to motherboard brackets. Position wires toward the Motorola Video Board and away from the motherboard area. Also, bad CRT's have been known to cause this symptom.
Motorola Video Board has been replaced and still have no video	Video Generator Module (VGM)	Replace U4 (74LS86) and U15 (74LS11)

NOTES:

1. These measurements should be observed with an oscilloscope, not a volt meter, as a volt meter will measure average duty cycle voltage and not represent the true peak-to-peak swing of the signal.

2. In some cases it may be necessary to replace both the Video Generator and the Motorola Video Board simultaneously to repair the system.

3. No thin horizontal/diagonal lines under high contrast settings is one way to check for sync. Turning brightness and contrast pots to maximum will allow you to view these lines.

4. U11 – Video Controller (MC6845).

E. THEORY OF OPERATION

The M3970 Series monitors are direct drive units requiring separate video, horizontal sync and vertical sync inputs. All are TTL compatible. Power supplied to the monitor is +12 V.

The monitor consists of a Video Amplifier, a Horizontal Driver, A Horizontal Output stage and two stages of Vertical Deflection (see Figure 1. Block Diagram).

Video Amplifier

The TTL compatible video signal, input at pin 8 of edge connector P1, is direct coupled via R2 to the base of the Video Amplifier Q1. R1 is used as the load resistor for the video signal source. The RC network (R4, R5 and C1) provides Q1 with increased gain at high frequencies by altering the collector-emitter load resistance ratio. At low frequencies, C1 appears as an "open" and only R4 is in the circuit. At higher frequencies, C1 "shorts", thereby shunting R4 with R5, lowering the emitter load resistance and increasing the emitter-collector resistance ratio. Therefore, the gain of Q1 increases. Approximate voltage gain of this stage is 25 V.

Resistor R3 provides the collector load for the video output signal. The amplified video is fed forward and direct coupled via R34 to the cathode of the CRT.

Horizontal Driver

The horizontal drive signal, input at pin 6 of P1, must be TTL compatible and a series of positive-going pulses of approximately 27.5 μsec duration (see Figure 2). In addition, the leading edge of the pulse may be coincident with the end of the video. If desired, the user may decide to delay the horizontal pulses (approximately 1.3 μsec) to attain centering of the video within the raster.

At the end of the video period, the horizontal drive signal goes positive and is coupled through C2 and R6 to the base of Horizontal Driver No. 2 (Q3). Q3 "turns on" drawing current through D1, R10 and C3. This action pulls the base of the Horizontal Output stage (Q4) low, forcing it into "cut-off". Approximately 27 μsec later, the negative-going trailing edge of the horizontal drive pulse switches Q3 off, which then allows Q2 to conduct. Base current is now provided to Q4 via the network R9, R10 and C3. The RC network, R10 and C3, is a speed-up network in the base circuit of Q4. It is used to increase the collector switching time of Q4.

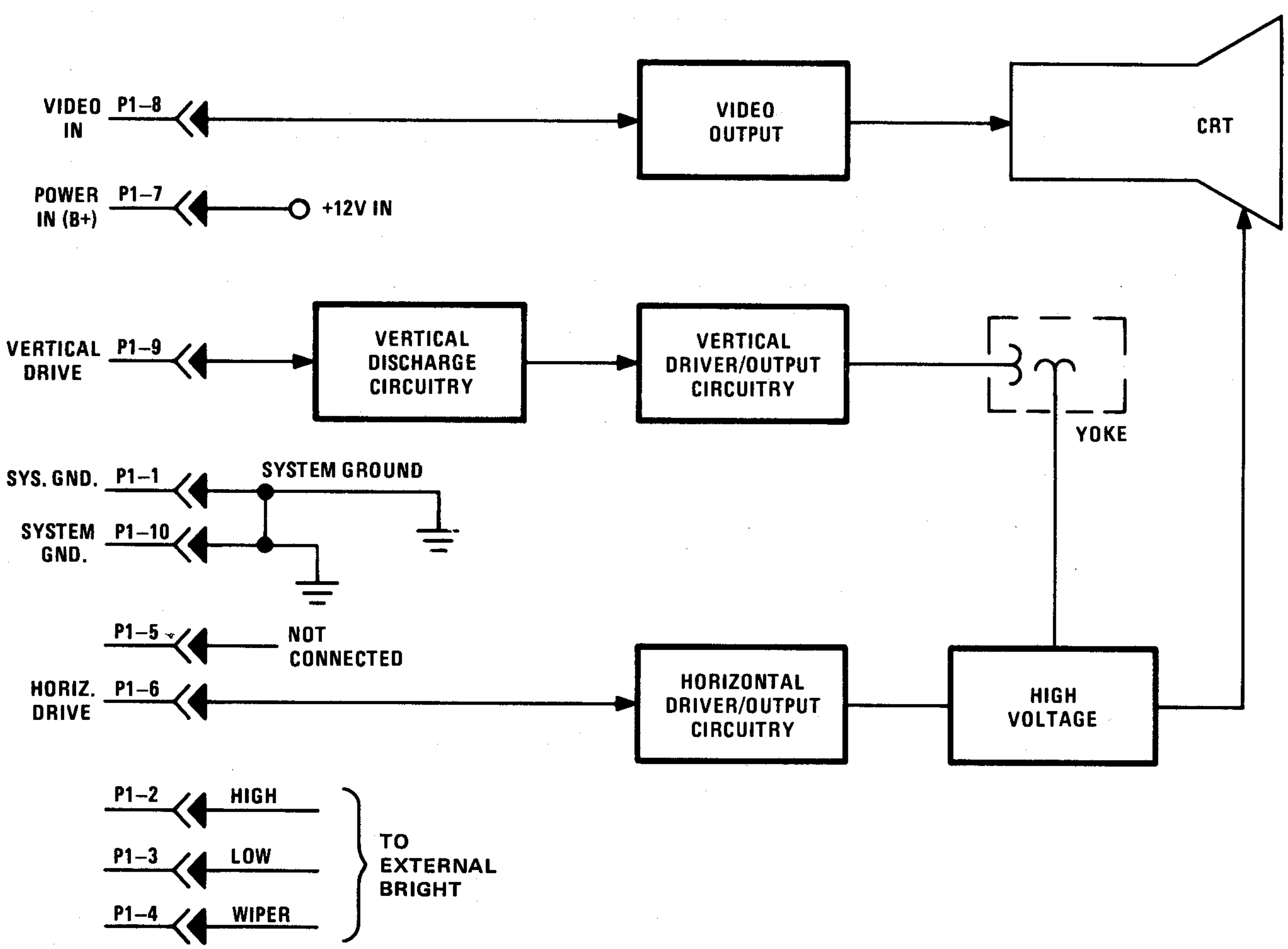


Figure 1. Block Diagram (Motorola and RCA)

At the end of the video period (horizontal drive going positive), the drive pulse at the base of Q4 goes low, forcing Q4 to cut off. This produces a retrace pulse occurring at the end of each line or sweep period that quickly drives the electron beam from the right to the left side of the screen.

Coincident with the retrace pulse, is the dissipation of the yoke current as determined by the LR time constant of the yoke, the primary windings of T1, and the action of D9. When the electron beam travels to about the center of the screen, Q4 turns on to form a current path from the +12V supply through the yoke (L2B)., the Horizontal Size (L3), and the Horizontal Linearity (L4) coils, to complete the raster line.

The retrace tuning capacitor, C4, forms a tuned circuit with the inductive components of the yoke, L2B. The linearity coil, L4, provides optimum horizontal linearity by shaping the deflection current per the amount of magnetic biasing as determined by the position of its core. The two RC networks, C17 and R39, and C16 and R38, provide damping for the coils L4 and L3, respectively, which eliminates any ringing effects in the circuits.

Horizontal Output Transformer

Transformer T1 produces secondary voltages via the auto transformer action of the primary winding. The transformer produces +60V, −110V, +300V and +12kV. The +60V supply is used as B+ for transistor Q1. At Q7, this voltage limits the peak voltage that appears at the collector, utilizing the electrical path through D5 and R27. The +60V and the −110V are applied across the brightness pot, R11. In addition, these voltages provide enough range to allow the blanking pulses to turn off the CRT beam during retrace.

The +300V source supplies the second grid, G2, of the CRT, in addition to the variable focus bleeder resistor. The +12kV supplies the second anode of the CRT with B+.

Vertical Deflection

The vertical drive signal, a negative-going short duration spike, is supplied to the unit via pin 9 of edge connector P1. This drive signal is direct coupled to the base of Q5 via R15. When the vertical drive signal is false or high, Q5 is cut off allowing C8 and C9 to charge toward +12V through the network of R17, R18, and D4. This charging action generates a linear positive-going ramp (sawtooth waveform) applied to the base of Q6, the Vertical Driver stage. When the vertical drive signal goes true or negative, Q5 conducts, discharging C8 and C9 to nearly zero volts. This action forms the retrace portion of the sawtooth waveform. Q6, an emitter follower configuration, transforms the high impedance of the sawtooth waveform into a low impedance drive for Q7, the vertical output stage.

The vertical output transistor, Q7, provides the required sawtooth waveform of current through vertical choke L1 and vertical yoke L2A. When Q7 is at minimum current flow during retrace, a large pulse voltage is developed as the yoke field collapses. The high voltage pulse is limited by D5 and R27 connected to the +60V source. The yoke coupling capacitor, C10, blocks any DC voltage to the yoke which can cause de-centering of the raster. The resistors R25 and R21 couple the emitter voltage of Q7 to the junction of C8 and C9. Because this path is resistive, the waveform coupled back will be integrated into a parabola by C8. This action pre-distorts the drive sawtooth and allows optimization of the vertical linearity adjustment.

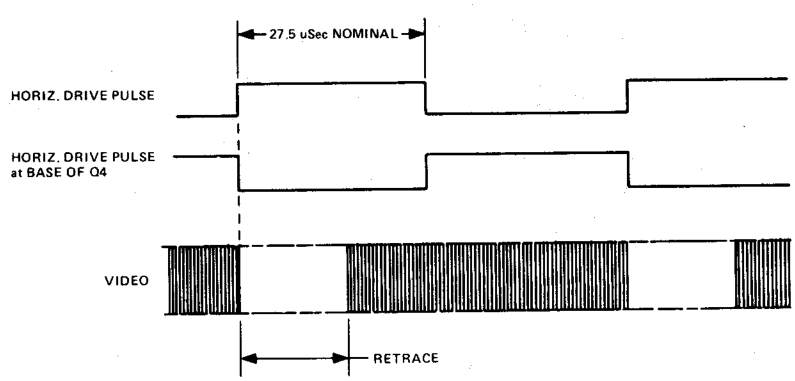


Figure 2. Horizontal Drive Signal (Motorola and RCA)

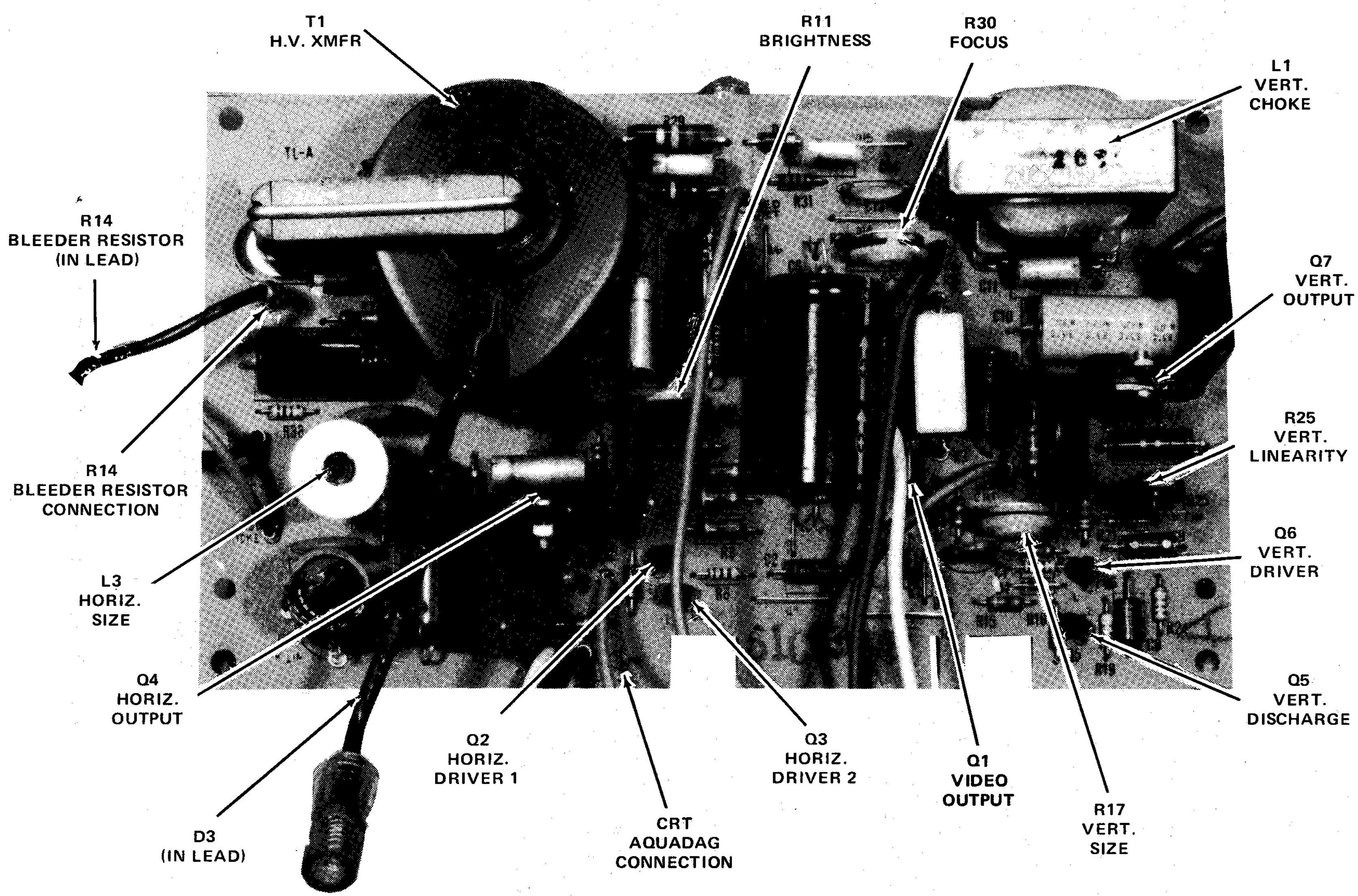


Figure 3. Model II Monitor [Display] P.C. Board — Component Location (Motorola)

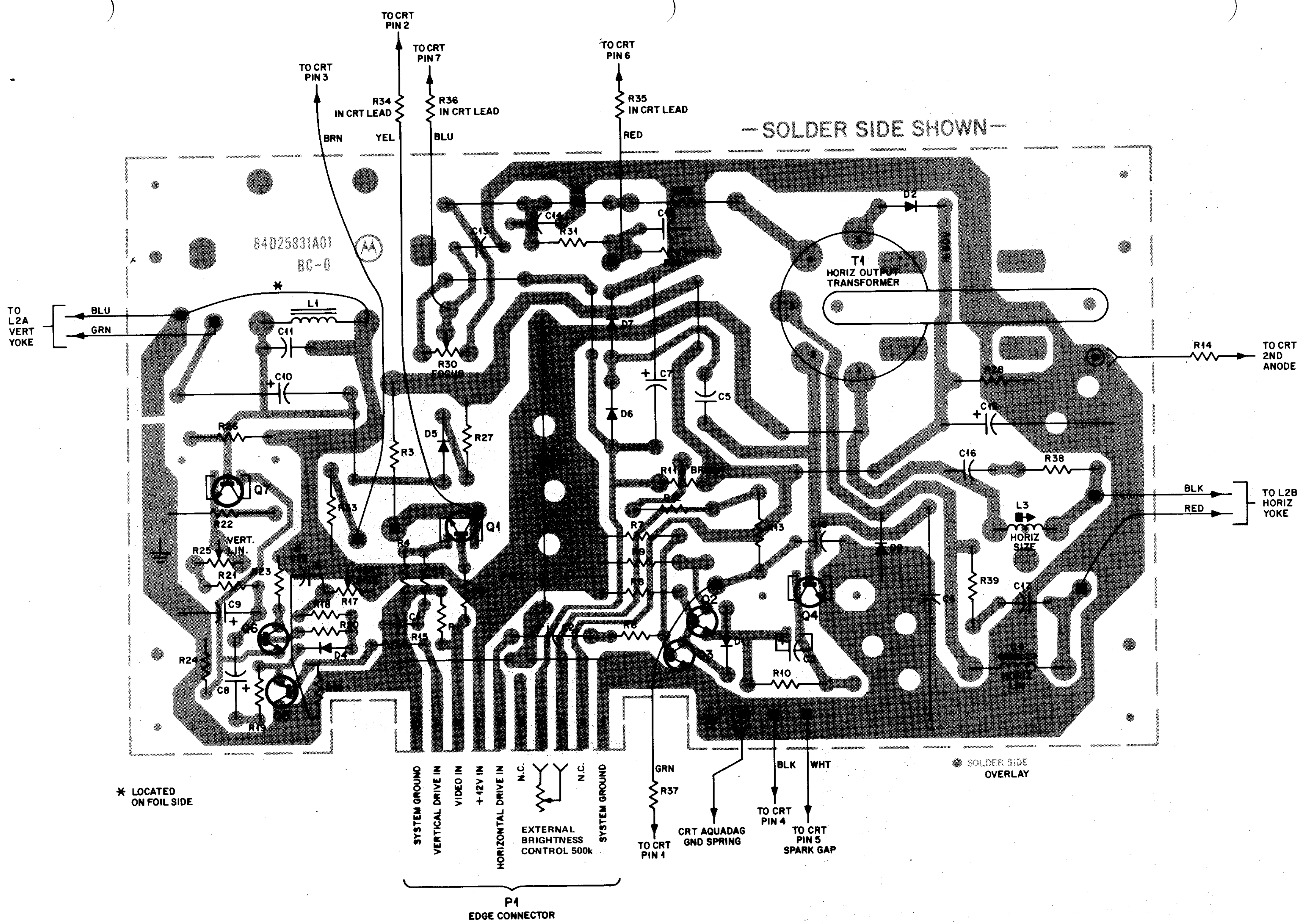


Figure 4. Model II Monitor [Display] P.C. Board — X-Ray View (Motorola)

F. INSTALLATION

Preliminary Checkout

The 12-inch CRT and associated components, which make up the basic M3970 video monitor kit, are mounted and shipped in a cardboard shipping carton. All components are properly interconnected for operation. Simply fabricate the mating plug for the edge connector on the rear of the monitor circuit card (refer to Figure 6).

To pretest the kit before final installation, remove the kit from the shipping carton or remove the kit from the pallet and open the cardboard shipping housing. (see Figure 5).

WARNING

A fire hazard exists if the monitor is operated in the shipping carton or on the cardboard shipping board for any length of time. Be sure that adequate ventilation is available to keep the ambient temperature in the monitor housing below +131°F (+55°C).

Cathode Ray Tube

As with any glass envelope vacuum tube, the danger of implosion is always present if dropped or mishandled. Even though the CRT used in this kit has integral implosion protection, handle the CRT with extreme care, and wear safety glasses. **Do not carry the CRT by its neck or apply excessive pressure.**

The CRT may be positioned with its high voltage cap (second anode connection) either left or right; however, be sure that the cap has a minimum of 1-inch clearance from any metal shield, bracket, etc.

To mount the CRT in its final operating location, use No. 8 type hardware and the holes in each corner of the CRT. After final installation, check to be sure that the CRT aquadag spring is positioned properly and grounded via a black wire to the monitor circuit card. Check to be sure that the bleeder resistor, R14, is connected to the ground lug (see Figure 4).

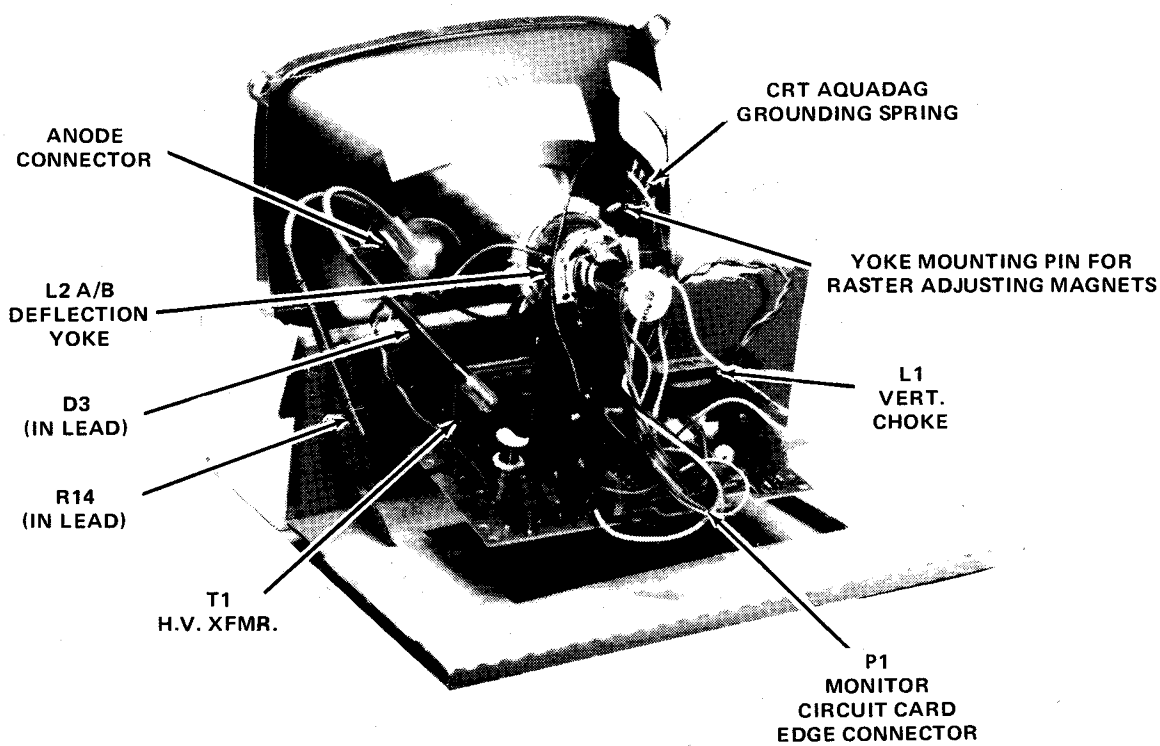


Figure 5. Model M3970 — Series Kits, Rear View (Motorola)

Monitor Circuit Card

The monitor circuit card is mounted vertically on the power supply bracket. Use four No. 6 type screws and hardware to secure the circuit card.

Do not allow any wires to lay on top of, or alongside any power transistor heat sinks on the circuit card. High heat dissipation could melt the wire insulation. In addition, be sure the yellow wire (CRT cathode connection) from the circuit card to pin 2 of the CRT socket does not lay near any metal or horizontal circuitry.

After final installation, be sure the CRT aquadag spring is connected via a black wire to the circuit card (refer to Figure 4).

Refer to section C. ADJUSTMENTS, and perform the steps as necessary.

– NOTE –

At the time of the initial installation procedure, it will be necessary to perform the Raster (Yoke) Adjustment Procedure.

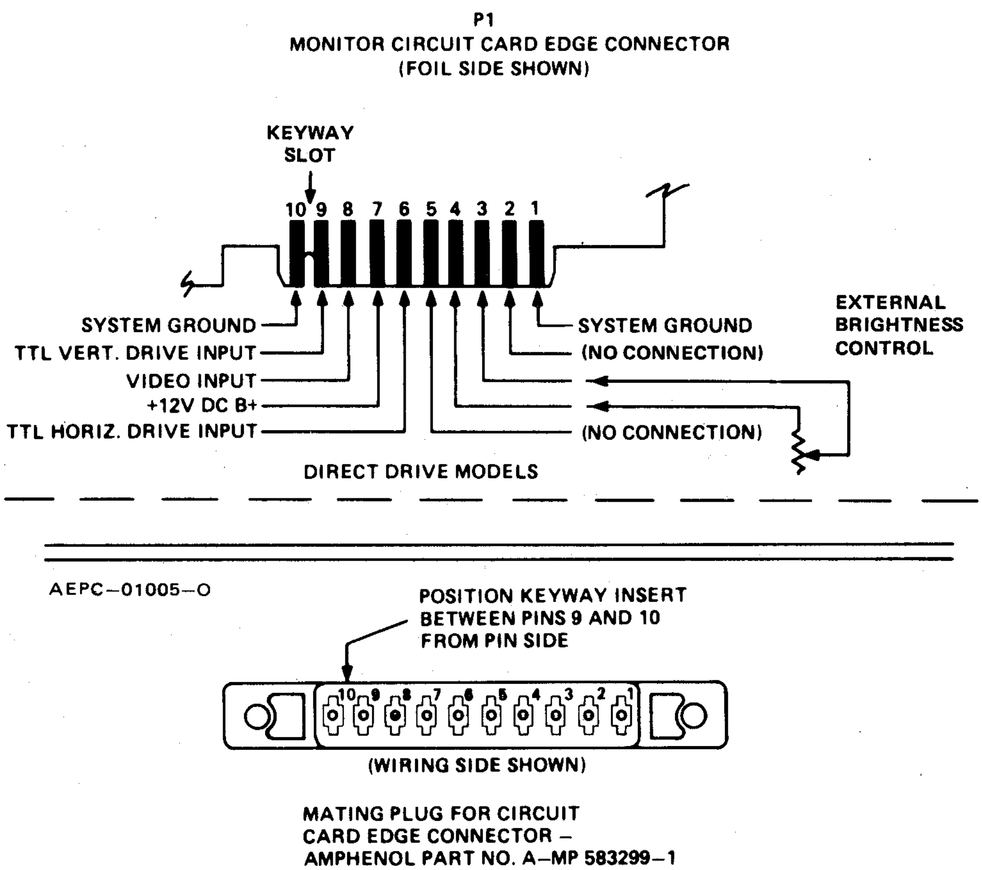


Figure 6. Monitor Circuit Card – Edge Connector (Motorola and RCA)

G. GENERAL SERVICING PRECAUTIONS

CAUTION

Before attempting to service the monitor, disconnect (or turn off) the external power supply; then, as an added precaution, discharge the CRT second anode before handling any high voltage components. In addition, be sure to observe all safety warnings and service notes in the front of this manual.

When it is necessary to disconnect the deflection yoke and/or the CRT socket leads, pull the small female pins straight out, **with no** back and forth rocking motion. This action will prevent, or at least, minimize the possibility of bending the male pins on the components and/or breaking the solder connections.

When disconnecting the H.V. rectifier, D3, pull it out of the high voltage lead holder slowly and carefully to prevent breaking or deforming the short rectifier lead.

Use caution around the heat sinks of the horizontal and vertical output transistors. The heat sinks are at the same potential as the transistor collectors. During normal operation with a signal input present, the horizontal heat sink has 130 volt P-P pulses and the vertical heat sink has 75 volt P-P pulses (with respect to system ground).

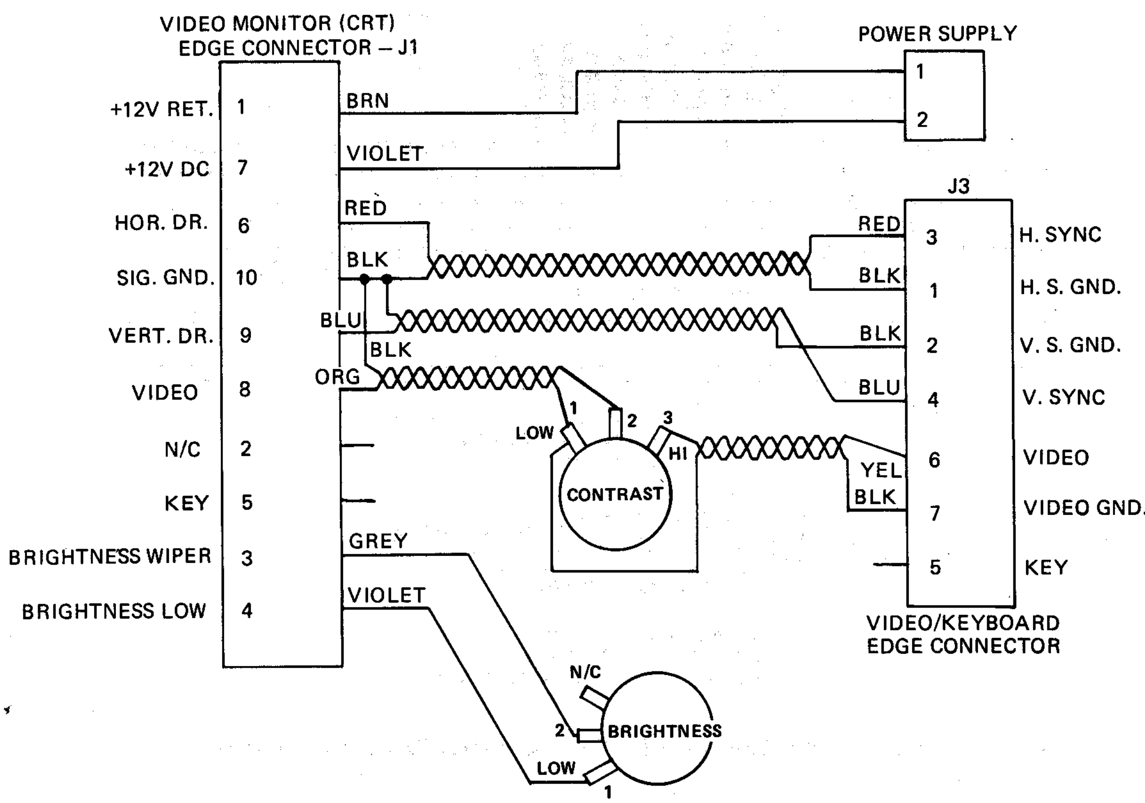


Figure 7. Video Wiring Harness (Motorola and RCA)

VIDEO MONITOR (MOTOROLA)
PARTS LIST

SYMBOL	DESCRIPTION	MANUFACTURER'S PART NUMBER	RADIO SHACK PART NUMBER
C1	0.001μF, Z5F, 100V, Disc	21S180B07	ACC102NCLP
C2	5μF, 15V, Tantalum	23S10218A31	ACC505QPTP
C3	0.68μF, 35V, Tantalum	23R29976A01	ACC684QGTP
C4	0.047μF, 200V, 10%, Poly	8S10072A44	ACC473QDEP
C5	0.047μF, 400V, 10%, Film	8R29959A02	ACC473QTGP
C6	2000μF, 35V, Electrolytic	23S10255A11	ACC208QGAP
C7	22μF, 160V, Electrolytic	23S10255A74	ACC226QNAP
C8	5μF, 15V, Tantalum	23S10218A31	ACC505QPTP
C9	5μF, 15V, Tantalum	23S10218A31	ACC505QPTP
C10	470μF, 16V, Electrolytic	23S102255A29	ACC477QDAP
C11	0.01μF, 400V, 10%, Film	8R29959A01	ACC103QTGP
C12	22μF, 160V, Electrolytic	23S10255A74	ACC226QNAP
C13	0.0027μF, Z5F, 500V, 20%, Disc	21S180C41	ACC272QUCP
C14	0.01μF, 400V, 10%, Film	8R29959A01	ACC103QTGP
C15	0.01μF, 400V, 10%, Film	8R29959A01	ACC103QTGP
C16	0.0022μF, Z5F, 500V, 10%, Disc	21S180C39	ACC222QUCP
C17	0.0022μF, Z5F, 500V, 10%, Disc	21S180C39	ACC222QUCP
C18	0.047μF, 400V, 10%, Film	8R29959A02	ACC473QTGP
C19	100μF, 16V, Electrolytic	23S10255A06	ACC107QDAP

COILS/CHOKES

SYMBOL	DESCRIPTION	MANUFACTURER'S PART NUMBER	RADIO SHACK PART NUMBER
L1	Coil, Vertical choke	25D25221A01	ACA8030
L2A/B	Yoke, Deflection	24D25830A01	ATA0770
L3	Coil, Width	24D25603A16	ACA8031
L4	Coil, Linear	24D25600A15	ACA8022

DIODES/RECTIFIERS

SYMBOL	DESCRIPTION	MANUFACTURER'S PART NUMBER	RADIO SHACK PART NUMBER
D1	Rectifier, Silicon, 91A02	48R191A02	ADX1330
D2	Rectifier, Silicon, 91A02	48R191A02	ADX1330
D3	Rectifier, H.V., D9H	48S137608	ADX1331
D4	Diode, Silicon, 2054	48R02054A00	ADX1332
D5	Rectifier, Silicon, 91A02	48R191A02	ADX1330
D6	Rectifier, Silicon, 91A02	48R191A02	ADX1330
D7	Rectifier, Silicon, 91A02	48R191A02	ADX1330
D8	Rectifier, Silicon, 91A05	48R191A05	ADX1333
D9	Rectifier, Silicon, 91A05	48R191A05	ADX1333

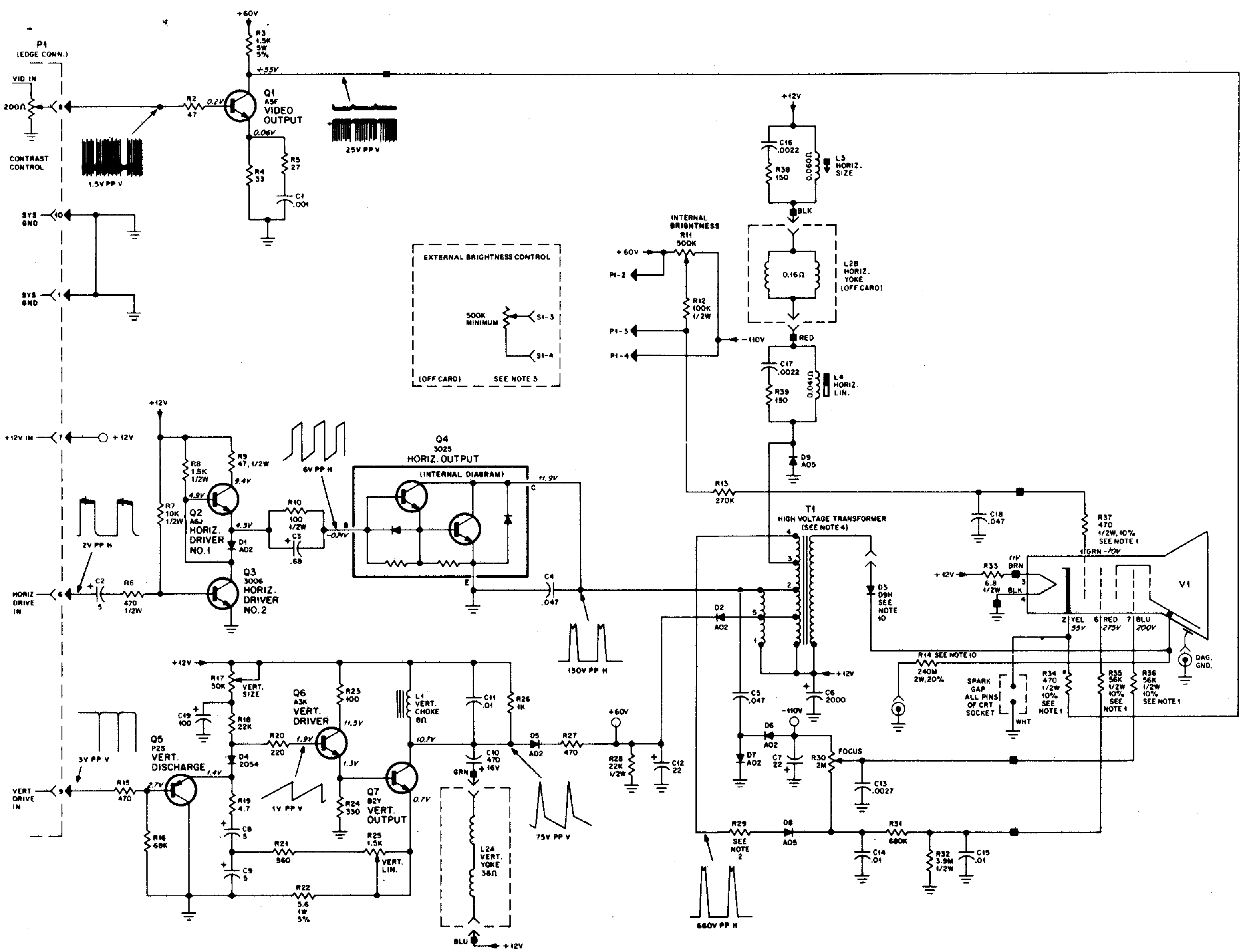
RESISTORS

Note: Only power or special resistors are listed. Use the description when ordering standard values of fixed carbon resistors up to 2 Watts.

SYMBOL	DESCRIPTION	MANUFACTURER'S PART NUMBER	RADIO SHACK PART NUMBER
R3	1.5K, 5W, 5%, Wire Wound	17–136062	AN0206FKB
R6	470 ohms, 0.5W, 10%, Composition	6–125C41	AN0169EFB
R7	10K, 0.5W, 5%, Film	————	AN0281EFB
R8	1.5K, 0.5W, 5%, Film	6–10164B32	AN0206EFB
R9	47 ohms, 0.5W, 5%, Film	6–10164B01	AN0099EFB
R10	100 ohms, 0.5W, 5%, Film	6–10164A78	AN0132EFB
R11	500K, Potentiometer	18D25245A07	AP-7038
R12	100K, 0.5W, 5%, Film	6–10164A80	AN0371EFB
R14	240M, 2W, 20%, Ceramic	6R29978A01	ARX0173

VIDEO MONITOR (MOTOROLA)
PARTS LIST (Cont'd)

SYMBOL	DESCRIPTION	MANUFACTURER'S PART NUMBER	RADIO SHACK PART NUMBER
	RESISTORS (Cont'd)		
R17	50K, Potentiometer	18D25245A20	AP-7039
R22	5.6 ohms, 1W, 5%, Composition	6–126B63	AN0052EGB
R25	1.5K, Potentiometer	18D25245A10	AP-7040
R28	22K, 0.5W, 5%, Film	6–10164B54	AN0311EFB
R29	18K, 1W, 5%	6–00126A79	AN0281FGB
R30	2M, Potentiometer	18D25245A12	AP-7041
R32	3.9M, 0.5W, 5%, Composition	6–125B36	AN0460EFB
R33	6.8 ohms, 0.5W, 5%, Film	6–10164L13	AN0054EFB
R34	470 ohms, 0.5W, 10%, Composition	6–125C41	AN0169EFB
R35	56K, 1.5W, 10%, Composition	6–125C91	AN0345FFB
R36	56K, 1.5W, 10%, Composition	6–125C91	AN0345FFB
R37	470 ohms, 0.5W, 10%, Composition	6–125C41	AN0169EFB
	TRANSFORMERS		
T1	Horizontal Output	24D25240A27	ATA0771
	TRANSISTORS		
Q1	A5F	48R137093	AMX4233
Q2	A6J	48R137172	AMX4234
Q3	MPS-A05	48R03006A00	AMX4235
Q4	BU807	48R03025A00	AMX4236
Q5	P2S	48R137127	AMX4237
Q6	A3K	48R134997	AMX4238
Q7	B2Y	48R137598	AMX4239
	MISCELLANEOUS		
V1	CRT, 12", 90°, P4	96R2500A15	AXX8002
	Anode Connector	42D25298A13	AJ6750
	CRT Socket	9D25241A08	AJ6751
	Yoke Magnet	59B25840A01	ART2572
	Aquadag Spring	41B25685B01	ARB6637
	1 inch Spacer	43S10865A01	AHB92U8
	Yoke Lead Terminal Lugs	29S10134A71	AJ6753
	Aquadag and Bleeder Wire Lugs	29S10134A55	AJ6752
	P.C. Panel	84–25561C93	AXX0312
	Picture Tube Socket	9–25241A08	AJ6751
	Heat Sink for Q4	26–25834B01	———
	Video Harness	———	AW2436

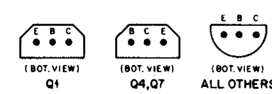


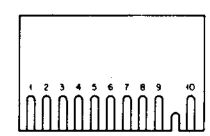
LEGEND:

- CIRCUIT CARD EDGE CONNECTION
- CIRCUIT CARD MALE PIN CONNECTION
- MALE PLUG CONNECTION
- FEMALE SOCKET CONNECTION
- REPRESENTS SOURCE OR DISTRIBUTION POINT FOR VOLTAGE VALUE INDICATED.
- REPRESENTS CONNECTION TO OFF CIRCUIT CARD LOCATION.

NOTES:

1. RESISTORS R34 THRU R37 ARE IN THEIR RESPECTIVE CRT LEAD.
2. VALUES FOR R29 ARE 10K 1W 10% OR 18K 1W 10%. REPLACE WITH APPROPRIATE VALUE.
3. SEE MANUAL FOR ALTERNATE WIRING DETAIL
4. THE DC RESISTANCE OF T1 IS AS FOLLOWS
   PIN 1 TO PIN 2 = 0.0925Ω
   PIN 1 TO PIN 3 = 0.401Ω
   PIN 1 TO PIN 4 = 6.27Ω
   PIN 1 TO ANODE LEAD = 676Ω
5. VOLTAGES MEASURED WITH CONTROLS SET FOR NOMINAL OPERATION; INPUT SIGNALS AS SHOWN.
6. DC VOLTAGES MEASURED WITH DVM.
7. WAVEFORMS TAKEN WITH 10 MHZ OSCILLOSCOPE REFERENCED TO SIGNAL GROUND, AND SYNCED AT VERTICAL (V) OR HORIZONTAL (H) RATE AS INDICATED.
8. COMPONENTS ENCLOSED BY DASHED LINES ARE MOUNTED OFF CIRCUIT CARD.
9. UNLESS OTHERWISE SPECIFIED
   ALL CAPACITORS ARE IN MICROFARADS
   RESISTORS ARE 1/4W, 5%.
10. COMPONENTS LOCATED IN HIGH VOLTAGE LEADS.





P1
EDGE CONNECTOR

1. SYSTEM GROUND
2. REMOTE BRIGHTNESS CONTROL (HIGH)
3. REMOTE BRIGHTNESS CONTROL (LOW)
4. REMOTE BRIGHTNESS CONTROL (WIPER)
5. N.C.
6. HORIZONTAL DRIVE IN
7. + 12V IN
8. VIDEO IN
9. VERTICAL DRIVE IN
10. SYSTEM GROUND

Figure 8. Model II Monitor [Display] Schematic Diagram (Motorola)

VIDEO MONITOR
(RCA)

H. FUNCTIONAL SPECIFICATIONS

General Information

The RCA Video Monitor uses the same interface circuitry as the Motorola Video Monitor. The Video Monitor is a 12" solid state monitor designed to display alphanumeric dot characters. It uses a 12-volt DC power input with an average power consumption of 12 watts. The monitor accepts separate video and vertical drive TTL level inputs.

Input and output connections for the monitor are made through a 10-pin circuit card edge connector. The inputs are video, horizontal drive, vertical drive, system ground and +12 volts.

A single circuit card with components mounted on one side is used. Schematic reference numbers are printed on both sides of the circuit card to aid in locating and identifying components for servicing.

Circuitry consists of one stage of video amplification, two stages of horizontal deflection processing, and three stages of vertical deflection processing.

SPECIFICATIONS

Cathode Ray Tube:	12" (305 mm) diagonal, 90^{o} deflection angle, 4 x 5 aspect ratio, P4 phosphor, integral implosion protection.
Environment:	
Operating Temperature:	41^{o}F to 131^{o}F (5^{o}C to 55^{o}C) ambient
Humidity:	95% non-condensing at 41^{o}F to 104^{o}F (5^{o}C to 40^{o}C)
Operating Altitude:	10,000 ft. (3048 meters) maximum
Power Input:	+12 VDC @ 1 amp, nominal
TTL Level	4 volts ±1.5 volts
Input Signals:	
Horizontal:	4 to 25 μsec, positive going
Vertical:	100 to 1400 μsec, negative going
Video:	positive white
Video Response:	
Bandwidth:	15 MHz, 3 dB Pulse rise time less than 30 nsec
Scanning Frequency:	
Horizontal:	15,600 Hz ±500 Hz
Vertical:	50/60 Hz
Horizontal Retrace:	10.5 μsec maximum
Vertical Retrace:	850 μsec maximum

SERVICE ADJUSTMENTS

NOTE

All measurements should be made using 12.0 VDC input. Measurements with the kine (CRT) attached will require that the ground strap from the kine be connected to the chassis to prevent transistor failures in the event of kine arcing.

FOCUS

Adjust the FOCUS control, F524 (Figure 9, Zone 2-A), for best overall focus.

VERTICAL SIZE

Adjust the VERTICAL SIZE control, R617 (Figure 9, Zone 3-B), to produce a vertical scan of approximately 6 inches (15.24 cm).

HORIZONTAL LINEARITY

Loosen the deflection yoke clamp and slide the linearity sleeve forward or to the rear to equalize character spacing on the left side of the screen to match character spacing on the right side of the screen (See Figure 10 for the location of the linearity sleeve).

WIDTH

Adjust the WIDTH control to produce a horizontal scan of approximately 8 inches (20.32 cm).

NOTE

Check the horizontal linearity prior to making the width adjustment.

CENTERING

Adjust the centering rings on the deflection yoke assembly to center the display on the screen, top to bottom and left to right.

HORIZONTAL HOLD

HORIZONTAL HOLD is accomplished by adjustment of the horizontal oscillator coil (Figure 9, Zone 4-D).

VERTICAL HOLD

Adjust the VERTICAL HOLD control, R612 (Figure 9, Zone 3-D).

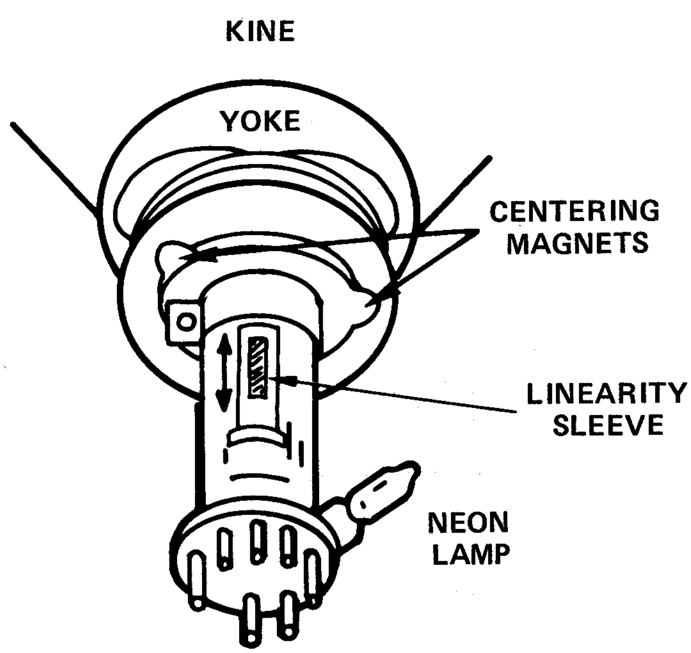


Figure 9.. Deflection Yoke Assembly (RCA)

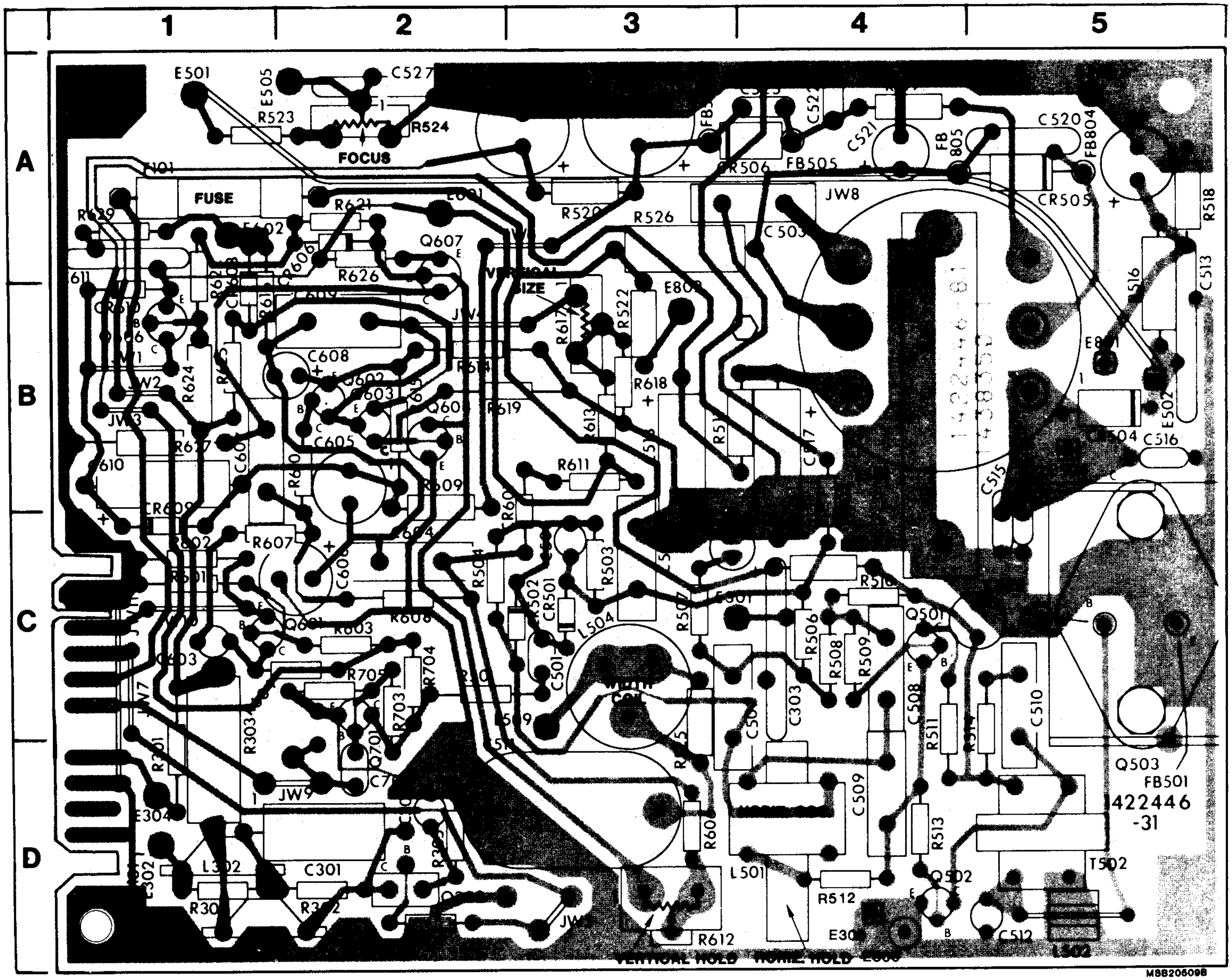


Figure 10. Model II Monitor [Display] P.C. Board – X-Ray View (RCA)

REPLACEMENT PARTS

PRODUCT SAFETY NOTE—Components marked with a (★) have special characteristics important to safety. Replacement of components marked with a (★) with anything other than the manufacturer's recommended replacement part may result in a safety hazard. Do not degrade the safety of the set through improper servicing or parts replacement.

VIDEO MONITOR KIT

CHASSIS ASSEMBLY

VDC-1

SYMBOL NO.	STOCK NO.	DRAWING NO.		DESCRIPTION
				CAPACITORS
C301	146763	1442134-66		.1 uf 10% 100V film
C302	147957	1491407-12m		220 pf 10% 50V Z5P disc
C303	137583	945304-125		.01 uf 20% 1000V disc
C501	145315	1491408-52m		2700 pf 10% 50V Z5P disc
C502	143879	1491407-91m		1000 pf 20% 50V Z5P disc
C503	134778	1472442-69		.033 uf 10% 100V film
C504	126425	1472442-66		.018 uf 10% 200V film
C505	142023	942966-224		36 pf 5% 500V N750 disc
C506	141028	1446666-151		5.6 uf 20V electrolytic
C507	134778	1472442-69		.033 uf 10% 100V film
C508	146012	1472442-65		.015 uf 10% 200V film
C509	126343	1472442-68		.027 uf 10% 100V film
C510	139441	1472442-63		.01 uf 10% 200V film
C511	138891	973991-83	★	
C512	143879	1491407-91m		1000 pf 20% 50V Z5P disc
C513	137583	945304-125		.01 uf 20% 1kV disc
C514	425666	945304-159	★	
C515	425666	945304-159	★	
C516	143029	945304-154	★	
C517	146113	984655-38		1 uf 150V electrolytic
C518	146113	984655-38		1 uf 150V electrolytic
C519	148889	1490001-17		1 uf 350V electrolytic
C520	141002	945802-37		390 pf 10% 500V N1500 disc
C521	141285	1446667-481		56 uf 10% 50V electrolytic
C522	120832	1420193-63		1000 pf 10% 500V disc
C523	141432	1490306-541		470 uf 25V electrolytic
C524	141163	1490306-441		330 uf 25V electrolytic
C525	120832	1420193-63		1000 pf 10% 500V disc
C527	137583	945304-125		.01 uf 20% 1kV disc
C528	142776	1490304-561		4.7 uf 50V electrolytic
C603	143879	1491407-91m		1000 pf 20% 50V Z5P disc
C604	134778	1472442-69		.033 uf 10% 100V film
C605	139285	1446668-241		220 uf 15V electrolytic
C606	139285	1446668-241		220 uf 15V electrolytic
C607	145359	1472442-60		5600 pf 10% 200V film
C608	137331	1446657-321		47 uf 6V electrolytic
C609	139444	1472442-75		.1 uf 10% 100V film
C610	145307	984655-42		.68 uf 80V electrolytic
C611	104205	1420193-69		3300 pf 10% 500V disc
C702	145740	1491407-21m		270 pf 20% 50V Z5P disc
				DIODES
CR501	119597	1471872-6		Horiz AFC
CR502	119597	1471872-6		Horiz AFC
CR504	140972	1476171-34		Damper
CR505	140971	1476171-33		+12V run
CR506	142569	1476171-31		+10V rectifier
CR606	119597	1471872-10		Silicon
CR607	119597	1471872-6		Silicon
CR608	119597	1471872-6		Silicon
CR609	119597	1471872-6		Silicon
CR610	119597	1471872-6		Silicon
F101	148886	1479891-6	★	Fuse — 2 amp
				BEADS
FB501	119971	1443391-2		Ferrite
FB502	119971	1443391-2		Ferrite
FB503	119971	1443391-2		Ferrite
FB504	119971	1443391-2		Ferrite
FB505	119971	1443391-2		Ferrite
FB506	119971	1443391-2		Ferrite
FB601	116761	1443391-1	★	Ferrite
				COILS
L301	137224	973966-54		39 uf
L302	140080	973966-65		22 uh
L501	148888	1474738-3		Horiz. hold
L502	145567	1479981-502		Choke bead
L504	148887	1478648-4		Width
				TRANSISTORS
Q302	141295	1417362-3		Video out
Q501	148907	1417346-3		Horizontal oscillator
Q503	140977	1417335-1		Horizontal output
Q601	142711	1417306-8		Vertical integrator
Q602	132830	1471112-8		Vertical oscillator
Q603	132830	1471112-8		Pre amp
Q604	139268	1417318-2		Vertical driver
Q606	141008	1417349-2		Vertical output top
Q607	137340	1417303-1		Vertical output bottom
Q701	142711	1417306-7		Horizontal sync separator
				RESISTORS
R303	149441	993260-157		2200 ohm 5% 3W ww
R516	512510	90496-231		1 meg ohm 5% 1W
R517	830147	993273-389	★	
R519	146774	993273-337	★	
R520	830010	993273-349	★	
R522	830A68	993273-345	★	
R523	430227	993218-469		1 meg ohm 5% 1/4W
R524	139062	1473359-26		control focus
R526	140983	946023-332	★	
R527	830010	993273-349	★	
R609	830033	993273-361	★	
R612	148892	1496161-10		control vertical hold
R613	148893	993218-483		3.9 meg ohm 5% 1/4W
R617	149178	1473359-47		control vertical size
R703	147588	993218-173		1.5 meg ohm 10% 1/4W
T501	148908	1465974-505	★	Transformer — high voltage rectifier assembly
T502	146777	1479977-3		Transformer — horizontal driver
	121134	1442419-4		Clamp — yoke
	148349	1465916-513		Socket — kine assembly
	148894	1463734-506	★	Yoke — deflection
				PICTURE TUBE
		12VCLP4	★	Picture tube

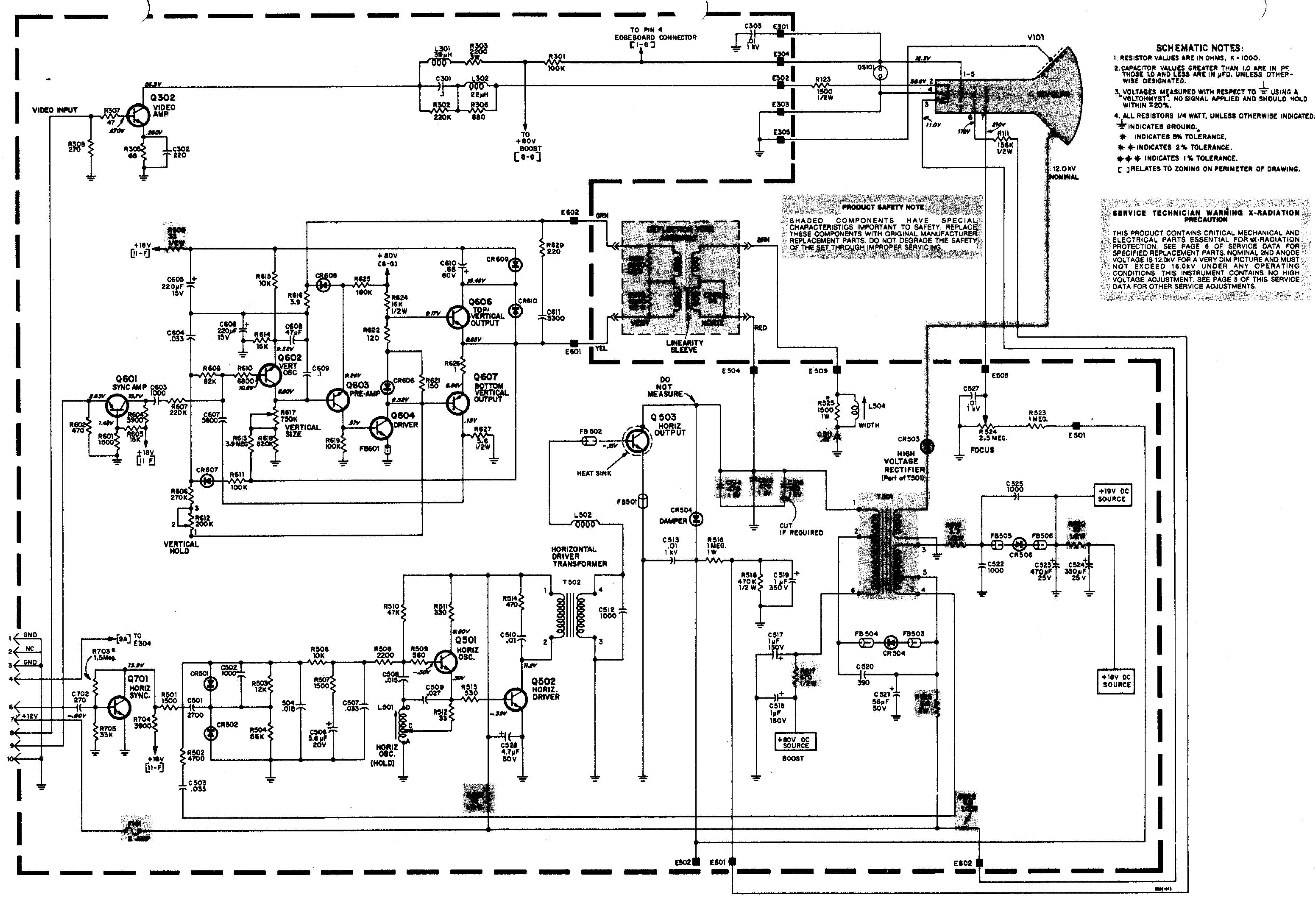


Figure 11. Model II Monitor [Display] Schematic Diagram (RCA)

SECTION VIII

FLOPPY DISK DRIVE

A. THEORY OF OPERATION

The floppy disk drive is a standard eight inch drive capable of supporting both single and double density recording formats. All of the disk drive control signals come from the floppy disk controller card. The drive contains two motors; one rotates the media at a constant speed while the other positions the read/write head over one of the 77 tracks. Electronics on the disk drive convert digital signals into read/write head signals and vice-versa.

NOTE: Models for overseas shipment may be configured with an AC Motor for the line voltage available in that country and may be fitted with a different drive pulley for 50 Hz line frequency.

B. JUMPER CONFIGURATION

All SA800 Drives:

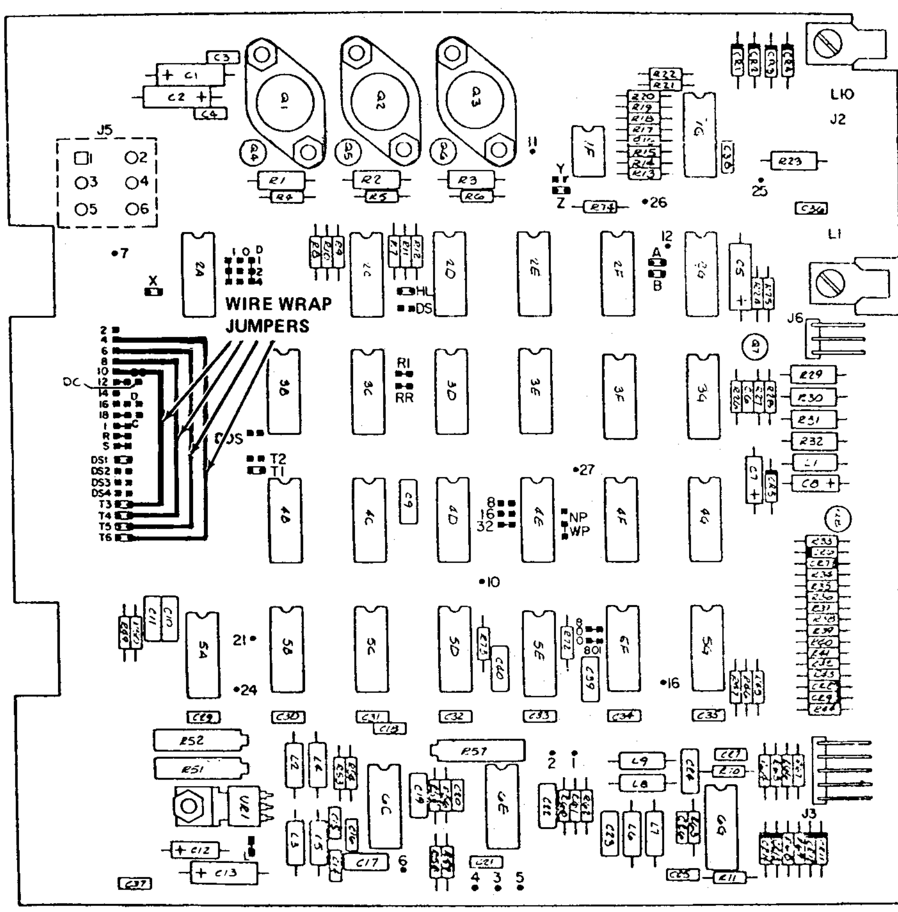
Refer to the **Shugart Maintenance Manual** and also see Figure 1 below.

1. Jumper "L" installed and oriented vertical as outlined on the silkscreen.
2. Jumpers installed on the following only! "A", "B", "C", "Z", "DS", "DC", "T1", "T2"

Disk Termination

When the Disk Expansion Unit is not connected to the Model II Computer, a special terminator must be connected to the Disk Expansion connector on the back of the Display Console. The terminator is a PC Board which provides jumpering to the termination resistors on the Computer's FDC PC Board. When using the computer in conjunction with a disk expansion unit, the terminator is removed and termination is provided on Drive No. 1 in the expansion unit.

The wire wrapped jumpers installed on pins 4, 6, 8, and 10, provide external termination along with the disk terminator. These jumpers must be installed as shown in the following illustration for proper termination when a disk expansion unit is not attached to the system.



Jumper Plug Installed as Shipped

• Test Point

Figure 1. SA 800/801 PCB Test Points and Component Locations.

SA800/801 DISK DRIVE MECHANICAL PARTS LIST

To find the Radio Shack Part Numbers of mechanical parts for the Disk Drive, find the required part using the illustrations and parts lists shown in the **Shugart Illustrated Parts Catalog** located in the back of this Technical Reference Manual. Using the appropriate part name and reference number, locate that part in the list below. You will note that in the first column below, the Figure Number and the Reference Number are listed, respectively.

Fig. & Ref. Number	Description	Radio Shack Part Number
3-15	Actuator, Head Load	AS-9109
1-6	Bearing, Spindle	ART-2298
1-9	Bearing, Spindle, Flanged	ART-2295
1-47	Belt	AB-6410
1-16	Boot, Rubber (for Motor Capacitor)	ART-2294
1-13	Bracket, Capacitor	ART-2291
4-3	Bumper	ART-2304
2-11	Carriage Spring Plate	ARB-6511
3-10	Cartridge Guide	ART-2293
1-1	Catridge Guide Assembly	ART-2288
1-31	Cartridge Guide Pivot	ART-2439
1-23	Clamp, Cable, 1/8" (3 mm)	ART-2299
1-45	Clamp, Cable, 3/16" (4.7 mm)	ART-2300
1-46	Clamp, Cable, 3/8" (9.5 mm)	ART-2301
2-3	Clamp, Mounting (for Stepper Motor)	ART-2309
1-53	Clip, Face Plate Mounting	ART-2438
1-49	Block, PCB Connector	AJ-6726
1-14	Connector, 3-pin Amp 7808	AS-6727
1-39	Deflector	ART-2306
1-25	Dust Cover Kit	ART-2296
3-1	Ejector Assembly	ART-2311
4-0	Front Plate Assembly	AZ-5074
1-34	Handle, Door	AH-6257
2-7	Head Carriage Assembly	AXX-0902
3-3	Hook, Spring	ART-2305
3-9	Hub Clamp Assembly	ART-2286
3-11	Hub Clamp Plate	ART-2289
1-10	Hub Assembly, Spindle	ART-2308
4-4	Latch Door	ART-2435
3-16	Latch Plate	ART-2436
3-14	LED Assembly	ART-2307
2-10	Load Button Assembly	ART-2302
1-20	Motor, Drive (Motor and Capacitor Assembly	AXX-4006
2-1	Motor, Stepper Assembly	AXX-4005
2-12	Nut, Carriage Load with cogs	ART-2314
1-2	Nut, 8-32	AHD-7146
1-44	Photo Transistor and Cable Assembly	AL-1042
2-4	Plate, Stepper Motor	ART-2292
----	Plug, Jumper or Shorting	AJ6731
1-21	Pulley, Drive Motor	ARA1338
1-4	Pulley, Spindle	ARA-2730
4-2	Push Bar Assembly	ART-2440
4-10	Screw, 4-40 x 1/4" (6.35mm) F/H	AHD-1488
1-37	Screw, 4-40 x 1/4" (6.35mm) SH/Hex	AHD-1489
1-27	Screw, 4-40 x 3/8" (9.5mm)	AHD-1490
1-50	Screw, 4-40 x 3/8" (9.5mm) R/H	AHD-1487
1-24	Screw, 6-32 x 5/16" (7.9mm)	AHD-1493
3-5	Screw, 6-32 x 5/16" (7.9mm)	AHD-1493
4-6	Screw, 6-32 x 5/16" (7.9mm)	AHD-1493

SA800/801 DISK DRIVE MECHANICAL PARTS LIST (cont'd)

Fig. & Ref. Number	Description	Radio Shack Part Number
4-6	Screw, 6-32 x 5/16" (7.9mm)	AHD-1493
1-51	Screw, 8-32 x 3/8" (9.5mm) SL/Hex/Wash	AHD-1492
1-19	Screw, 8-32 x 3/4" (19mm)	AHD-1491
2-6	Screw, Cap 2-56 x 1/4" (6.35mm)	AHD-1495
1-33	Screw, Cartridge Guide Assembly	AHD-1494
1-25	Screw, Dust Cover	AHD-1496
1-22	Screw, Set, 6-32 x 1/8" (3mm)	AHD-0031
1-42	Screw, Tapping, 8 x 1/2" (12.7mm)	AHD-3252
4-8	Snatch	ART-2437
1-41	Spacer	ART-2310
1-7	Spacer, Spindle–Long	ART-2297
1-5	Spacer, Spindle–Short	ART-2290
2-15	Spacer, Stepper Plate	ART-2313
1-30	Spring Assembly	ARB-6513
1-32	Spring, Bias	ARB-6510
3-2	Spring, Clamp Ejector	ARB-6512
1-26	Spring, Guide Assembly	ART-2285
3-8	Spring, Hub Clamp	ARB-6507
4-5	Spring, Latch Interlock	ART-2312
2-13	Spring, Pre-load	ARB-6508
1-8	Spring, Spindle	ARB-6509
1-28	Track Ø Detector	AL-1041
2-8	Track Ø Flag	ART-2287
2-5	Track Ø Stop	ART-2303
2-17	Washer, Spring, #6	AHD-8445
1-3	Washer, Spring, #8	AHD-8444
3-17	Write Protect Assembly	ART-2284

SECTION IX

AA11080 POWER SUPPLY

A. FUNCTIONAL SPECIFICATIONS

The power supply for the TRS-80 Model II is a 150 watt, switching power supply. The Printed Circuit Board is mounted to an open L-shaped bracket which provides heatsinking as well as mounting surfaces. Line input to the power supply module is made through an amp wafer with locking 3-pin PCB socket header.

Pin 1	Line - Neutral
Pin 2	Blank
Pin 3	Line - Live

Outputs are taken from an amp wafer with locking 15-pin PCB socket header.

Pin 1	-12V
Pin 2	-12V
Pin 3	Common
Pin 4	Common
Pin 5	Common
Pin 6	Common
Pin 7	Common
Pin 8	+5V
Pin 9	+5V
Pin 10	Common
Pin 11	+5V
Pin 12	+5V
Pin 13	+24V
Pin 14	+12V
Pin 15	+12V

In theory, the power supply rectifies the AC line to DC then chops it at 20 kHz. The chopped DC voltage is then transformed to the required output voltages and rectified to low voltage isolated DC. Feedback loops are provided for voltage regulation and over current protection.

The power supply may be jumper selected for either of the following ratings:

Vin - 95 to 135VAC @ 47 to 63Hz input frequency
or - 190 to 270VAC @ 47 to 63Hz input frequency

The power supply module can withstand the following maximum ratings:

Vin (AC continuous) - 140V input select 115V
or - 280V input select 230V

Short Circuit, any output - indefinite

B. TROUBLESHOOTING

1. Equipment for Test Set-Up:

a. Isolation Transformer (minimum of 500 VA rating) —

> ***CAUTION***
>
> Dangerously high voltages are present in this power supply. For the safety of the individual doing the testing, please use an isolation transformer. The 500 VA rating is needed to keep the AC waveform from being clipped off at the peaks. These power supplies have peak charging capacitors and draw full power at the peak of the AC waveform.

b. 0-140V Variable Transformer (Variac) — Used to vary input voltage. Recommend 10 amp, 1.4 KVA rating, minimum.

c. Voltmeter — Need to measure DC voltages to 50 VDC and AC voltages to 200 VAC. Recommend two digital multimeters.

d. Oscilloscope — Need X10 and X100 probes.

e. Load board with Connectors — See Table 1 for values of loads required. The entry on the table for Safe Load Power is the minimum power ratings for the load resistors used.

NOTE: Because of its design, this power supply must have a load present or damaging oscillations may result. **Never test the power supply without a suitable load!**

f. Ohmmeter

2. Set-Up Procedure:

Set-up as shown in Figure 1. You will want to monitor the input voltage and the output voltage of the regulated bus, which is the +5 output, with DVM's. Also monitor the +5 output with the oscilloscope using 50mv/div sensitivity. The DVM monitoring the +5 output can also be used to check the other outputs. See text of section C. for test points within the power supply.

Table 1. LOAD BOARD VALUES

OUTPUT	MIN LOAD	LOAD R	SAFE LOAD POWER	MAX LOAD	LOAD R	SAFE LOAD POWER
+5	2.15A	2.32 ohm	20W	8.6A	0.58 ohm	80W
+12	1.25A	9.6 ohm	30W	4.5A	2.67 ohm	100W
+24	0	0	0	1.7A	14.12 ohm	80W
-12	0.05A	2.40 ohm	1W	0.2A	60 ohm	5W

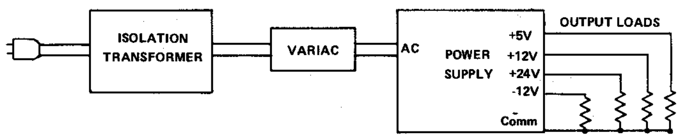


Figure 1. Test Lay-out

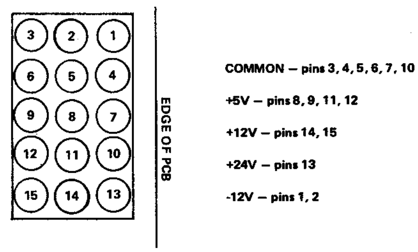


Figure 2. Output Connector (S2)

3. **Visual Inspection:**

   Check power supply for any broken, burned, or obviously damaged components. Visually check fuse, if any question check with ohmmeter.

4. **Start-Up:**

   Load power supply with minimum load as specified in Table 1. Bring up power slowly with Variable Transformer while monitoring the +5 output with the oscilloscope and DVM. Supply should start with approximately 40-60 VAC applied, and should regulate when 95 VAC is reached. If output has reached 5 volts, do a performance test as shown in section D. If there is no output, refer to section C.

5. **Bracket Removal:**

   The main PCB is held to the bracket with five bolts and uses spacers with each one to keep the PCB from contacting the bracket. Rectifier heat-sink is held to the bracket with three bolts run directly into PEM-nuts.

C. NO OUTPUT

1. **Check Fuse:**

   If fuse is blown, replace it but do not apply power until cause of failure is found.

2. **Preliminary Check on Major Primary Components:**

   Check diode bridge (BR1), power transistor (Q1), and catch diode (D3) for shorted junctions. If any component is found shorted, replace it.

3. **Preliminary Check on Major Secondary Components:**

   Using an ohmmeter from an output that is common to each output and with output loads disconnected, check for shorted rectifiers or capacitors. If the +5 is shorted, also check crowbar SCR (SCR 1) and zener diode (Z1).

4. **Check for B+:**

   Set up power supply and attach the X100 scope probe ground to the negative terminal of the large input capacitor nearest to Q1. Slowly turn up power and check for B+ on the jumper marked F2 near the power transistor. With input at 95 VAC, this point should be between 280 and 300 VDC. If this is not correct, check BR1, the fuse, and if necessary, R5, D1, and D2. Also check input capacitors C5 and C6.

5. Check Q1 Waveforms

Using X100 probe on case of TO-3 package of Q1, check collector waveform. Transistor should be switching. The correct waveform is shown in Figure 3. If switching is not present, check for shorted junctions on Q1. If OK, check the base waveform.

The base of Q1 (looking under the PCB) is the pin from the center of Q1, closest to the PCB corner. The correct waveform is shown in Figure 4. If the waveform is not there, check for clock pulses which will show as spikes of approximately 2 volts magnitude every 50 μsec. If these spikes are not there, then control module should be replaced, especially if no other component failures can be found.

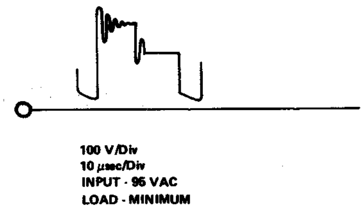


Figure 3. Q1 Collector Waveforms

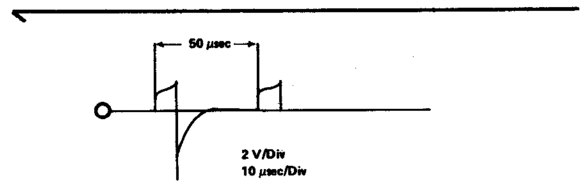


Figure 4. Q1 Base Waveforms

D. PERFORMANCE TEST

Each of these test conditions should be set-up and noted to be within the limits specified in Table 2.

Test	Input	+5 Load	+12 Load	+24 Load	-12 Load
1	95VAC	Max	Max	Max	Max
2	135VAC	Max	Max	Max	Max
3	*135VAC	Max	Max	Max	Max
4	135VAC	Min	Min	Min	Min
5	95VAC	Min	Min	Min	Min

*On test 3, input voltage should be varied over full range to search for instability after correct outputs are noted at 135 VAC.

TABLE 2. VOLTAGE AND RIPPLE SPECIFICATIONS

OUTPUT	MIN	MAX	NO LOAD	RIPPLE
+5	4.90V	5.10V	-	50mV P-P
+12	11.40V	12.60V	-	100mV P-P
+24	21.20V	26.40V	30.0V	250mV P-P
-12	-11.40V	-12.60V	-	50mV P-P

OPERATING CHARACTERISTICS

		MIN	TYP	MAX	UNITS
Operating Voltage Range		95	115	135	VAC
		190	230	270	VAC
Line Frequency		47	50/60	63	Hz
Output Voltages	VO1	4.90	5.00	5.10	V
	VO2	11.40	12.00	12.60	V
	VO3	21.20	24.00	26.40	V
	VO4	-11.40	-12.00	-12.60	V
VO3, no load tolerance		21.20	–––	30.00	V

NOTE: VO1/VO2 specified for balanced loads.
All voltages measured at connector.

		MIN	TYP	MAX	UNITS
Output Loads	IO1	2.15	4.3	8.6	A
	IO2	1.25	2.25	4.5	A
	IO3	0	1.3	1.7	A
	IO4	0.05	0.1	0.2	A
OCP, Current Limit	ICL1	9.0	11.0	14.0	A
	ICL2	4.6	5.5	7.0	A
	ICL3	1.8	2.5	3.5	A
	ICL4	–––	1.0	2.0	A

NOTE: VO4 is a thermally protected IC regulator.

		MIN	TYP	MAX	UNITS
OVP, Crowbar VCB1		5.94	6.25	7.00	V
Output Resistance	RO1	–––	2.3	–––	M ohm
	RO2	–––	130	–––	M ohm
	RO3	–––	590	–––	M ohm
	RO4	–––	–––	–––	–––––
Output Noise	VO1	–––	–––	50	mV p-p
	VO2	–––	–––	100	mV p-p
	VO3	–––	–––	250	mV p-p
	VO4	–––	–––	50	mV p-p
Efficiency		70	80	–––	%
Load Transient VOS		–––	0.3	–––	V
VO1, 25% to 75% TROS		–––	1.0	–––	mSec
Load Step	VUS	–––	0.3	–––	V
	TRUS	–––	1.0	–––	mSec
Hold Up Time:					
Full Load	Lo Line	10	18	–––	mSec
Full Load	Nom Line	16	30	–––	mSec

OPERATING CHARACTERISTICS (cont'd)

		MIN	TYP	MAX	UNITS
Insulation Resistance					
Input to Output		100	1000	---	M ohm
Input to Ground		100	1000	---	M ohm
Output to Ground		100	1000	---	M ohm
Isolation					
Input to GND and Op		4.24	---	---	KVDC
Line Conducted EMI					
(Reference VDE 0875)	0.15 to 0.5 MHz	---	1.0	---	mV
	0.5 to 5 MHz	---	0.5	---	mV
	5 to 50 MHz	---	0.5	---	mV

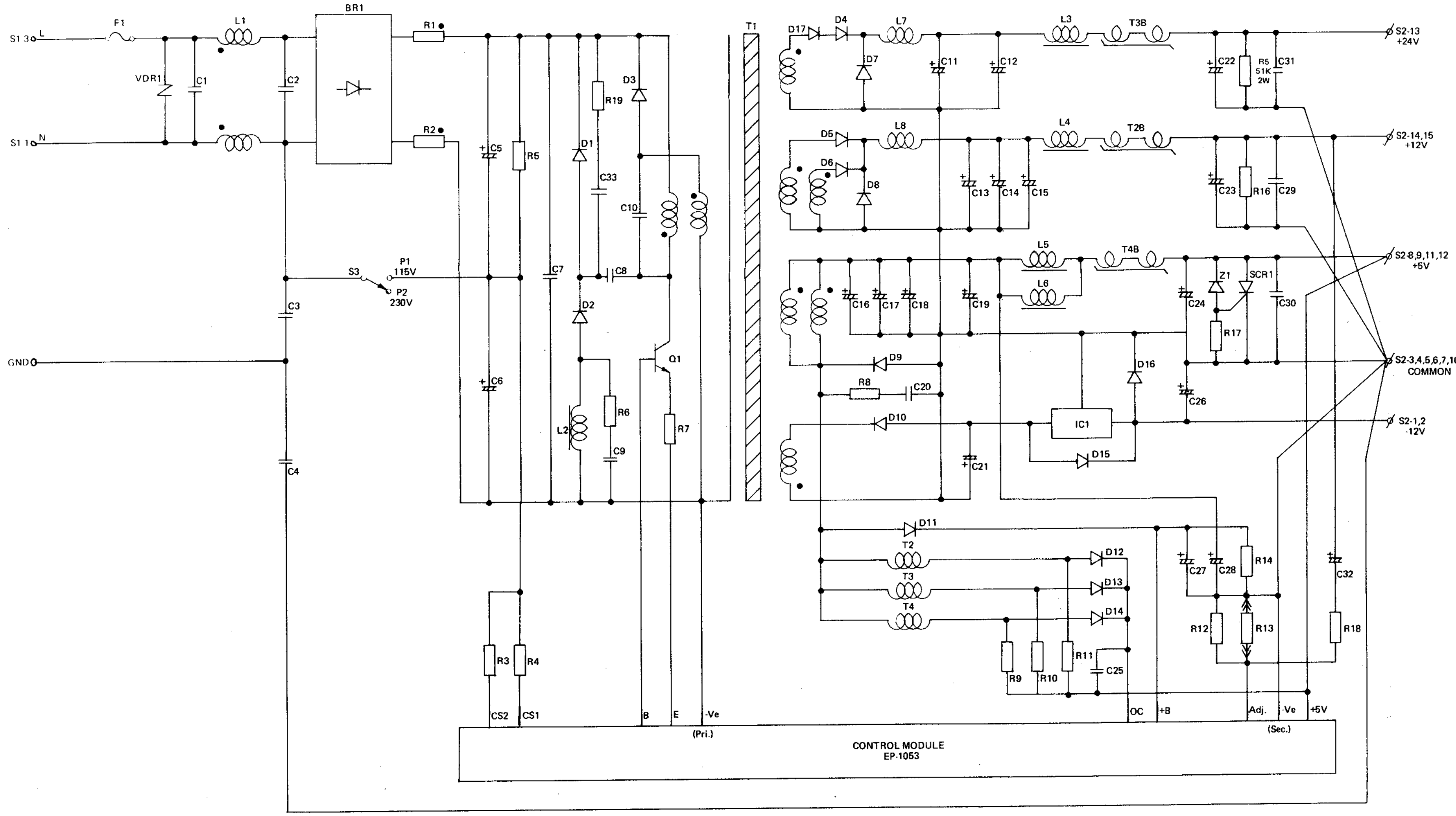


Figure 5. AA11080 Power Supply Schematic

SECTION X

CARD CAGE and MOTHERBOARD

A. DESCRIPTION

The card cage provides mechanical support for and electrical connections to the digital electronics boards. The main component of the card cage is the Motherboard, which holds eight 80-pin card edge connectors.

Four of these connectors are used for the boards required by the basic system. These cards should be in the following order, (slot one being the connector closest to the power supply):

CPU	Slot 1
FDC	Slot 2
Memory	Slot 3
Video	Slot 4

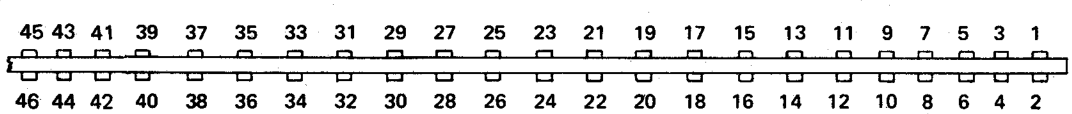
If your system is shipped with 64K of RAM you will have four connections open for future additions. If your system is shipped with 32K of RAM, you can add another 32K by returning the unit to Radio Shack. Another 32K board will be added to the card cage in Slot 5, leaving still three connectors open for future expansion of your system.

CARD CAGE AND MOTHERBOARD PARTS LIST

SYMBOL	DESCRIPTION	QUANTITY	MANUFACTURER'S PART NUMBER	RADIO SHACK PART NUMBER
		CAPACITORS		
C1	470μF, 16V, electrolytic, radial	1	8327471	ACC477QDAP
C2	470μF, 16V, electrolytic, axial	1	8317471	ACC477QDAA
C3	470μF, 16V, electrolytic, axial	1	8317471	ACC477QDAA
C4	0.1μF, 50V, monolithic, axial	1	8374104	———
C5	0.1μF, 50V, monolithic, axial	1	8374104	———
C6	0.1μF, 50V, monolithic, axial	1	8374104	———
		HARDWARE		
	Nut, Hex, #4	6	8579012	AHD-7166
	Screw, 4-32 x ½" (12.7mm)	6	8569033	AHD-1542
	Screw, 6 x ¼" (6.35mm)	4	8569040	AHD-1547
	Washer, flat	12	8589002	AHD-8500
	Washer, flat, nylon, #8	1	8589022	AHD-8519
		RESISTORS		
R1-17	2.2K, ¼W, 5%	17	820722	AN0216EEC
RP1	Resistor Pak, 390 ohm	1	829002	ARX-0167
RP2	Resistor Pak, 390 ohm	1	829002	ARX-0167
		MISCELLANEOUS		
	Bracket, PC Left side	1	8729015	ART-2686
	Bracket, PC Right side	1	8729011	ART-2682
	Card Guide	1	8719052	AHB-9439
	Card Guide Support	1	8729013	ART-2684
	Connector, 80-pin card edge	1	8509014	AJ-6762
J1	Connector, power	1	8509015	AJ-6763
	Motherboard Assembly	1	8893430	AXX-0500

MOTHERBOARD (80-PIN BUS) SIGNAL DESCRIPTION

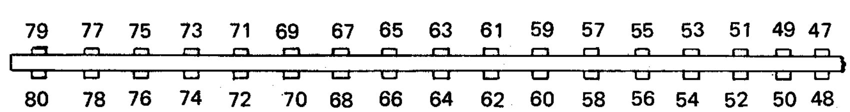
PIN	SIGNAL NAME	DESCRIPTION
1	USERØ	User Definable
2	USER1	User Definable
3	GND	Power Ground
4	GND	Power Ground
5	+12V	Positive 12-Volt Power
6	+12V	Positive 12-Volt Power
7	GND	Power Ground
8	GND	Power Ground
9	+5V	Positive 5-Volt Power
10	+5V	Positive 5-Volt Power
11	INTRQ*	Maskable Interrupt Request (in)
12	NMIRQ*	Non-Maskable Interrupt Request (in)
13	IEIN	Interrupt Enable In (in)
14	IEOUT	Interrupt Enable Out (out)
15	BAKIN*	Bus Acknowledge In (in)
16	BAKOUT*	Bus Acknowledge Out (out)
17	BUSRQ*	Bus Request (in)
18	SYNC*	Z-80 M1 (Indicates Op-Code Fetch) (out)
19	RD*	Read in Progress (out)
20	WR*	Write in Progress (out)
21	MEMCYC*	Z-80 MEMRQ (Memory Cycle in Progress) (out)
22	IOCYC*	Z-80 IORQ (I/O Cycle in Progress) (out)
23	AØØ*	Address Bit Ø Inverted (out)
24	AØ1*	Address Bit 1 Inverted (out)
25	AØ2*	Address Bit 2 Inverted (out)
26	AØ3*	Address Bit 3 Inverted (out)
27	AØ4*	Address Bit 4 Inverted (out)
28	AØ5*	Address Bit 5 Inverted (out)
29	AØ6*	Address Bit 6 Inverted (out)
30	AØ7*	Address Bit 7 Inverted (out)
31	AØ8*	Address Bit 8 Inverted (out)
32	AØ9*	Address Bit 9 Inverted (out)
33	A1Ø*	Address Bit 10 Inverted (out)
34	A11*	Address Bit 11 Inverted (out)
35	A12*	Address Bit 12 Inverted (out)
36	A13*	Address Bit 13 Inverted (out)
37	A14*	Address Bit 14 Inverted (out)
38	A15*	Address Bit 15 Inverted (out)
39	RES	Reserved for System Expansion
40	DISRO*	Disable RAM Output (in)
41	XFERRQ	DMA Transfer Request (in)
42	KBIRQ*	Keyboard Interrupt Request (in)
43	SELECT*	Board Selected (out)
44	CLOCK	4MHz System Clock (out)
45	REFRSH*	Z-80 RAM Refresh Signal (out)
46	8MHz	Times Two System Clock (out)



MOTHERBOARD (80-PIN BUS) SIGNAL DESCRIPTION (cont'd)

PIN	SIGNAL NAME	DESCRIPTION
47	RTC	Real Time Clock Heart Beat (3Ø or 6ØHz) (out)
48	WAIT*	Z-80 Wait Request (in)
49	GND	Power Ground
50	GND	Power Ground
51	DATØ*	Data Bit Ø Inverted (input/output)
52	DAT1*	Data Bit 1 Inverted (input/output)
53	DAT2*	Data Bit 2 Inverted (input/output)
54	DAT3*	Data Bit 3 Inverted (input/output)
55	DAT4*	Data Bit 4 Inverted (input/output)
56	DAT5*	Data Bit 5 Inverted (input/output)
57	DAT6*	Data Bit 6 Inverted (input/output)
58	DAT7*	Data Bit 7 Inverted (input/output)
59	RES	Reserved for System Expansion
60	RES	Reserved for System Expansion
61	RES	Reserved for System Expansion
62	RES	Reserved for System Expansion
63	RES	Reserved for System Expansion
64	RES	Reserved for System Expansion
65	RES	Reserved for System Expansion
66	RES	Reserved for System Expansion
67	RESET*	System Reset (out)
68	HALT*	Z-80 Halt Indication (out)
69	GND	Power Ground
70	GND	Power Ground
71	+5V	Positive 5-Volt Power
72	+5V	Positive 5-Volt Power
73	GND	Power Ground
74	GND	Power Ground
75	-12V	Negative 12-Volt Power
76	-12V	Negative 12-Volt Power
77	+12V	Positive 12-Volt Power
78	+12V	Positive 12-Volt Power
79	GND	Power Ground
80	GND	Power Ground

*Indicates an inverted signal, or an active low signal.



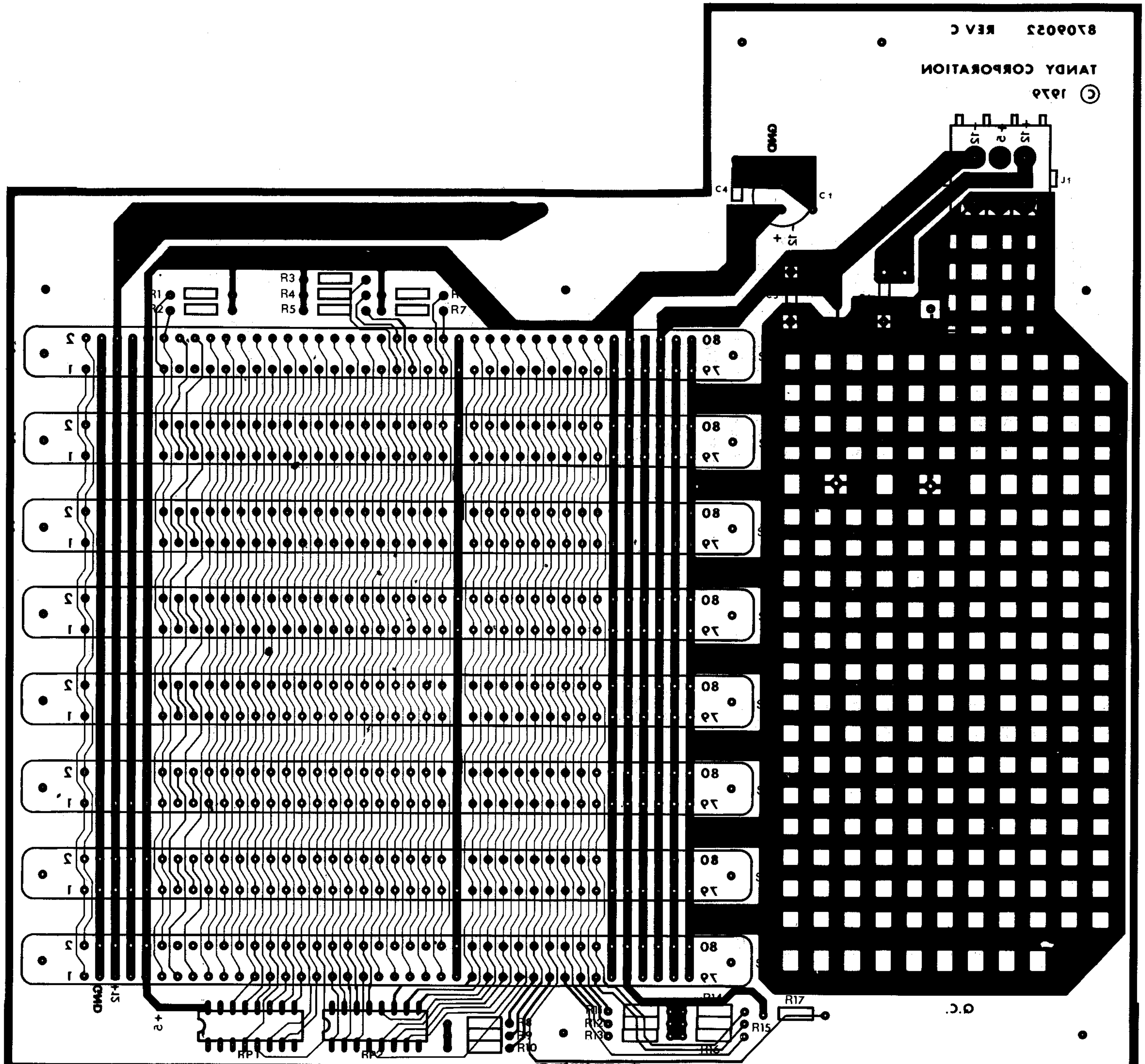


Figure 1. X-Ray View of Motherboard Pr... d Circuit Board — Component Side

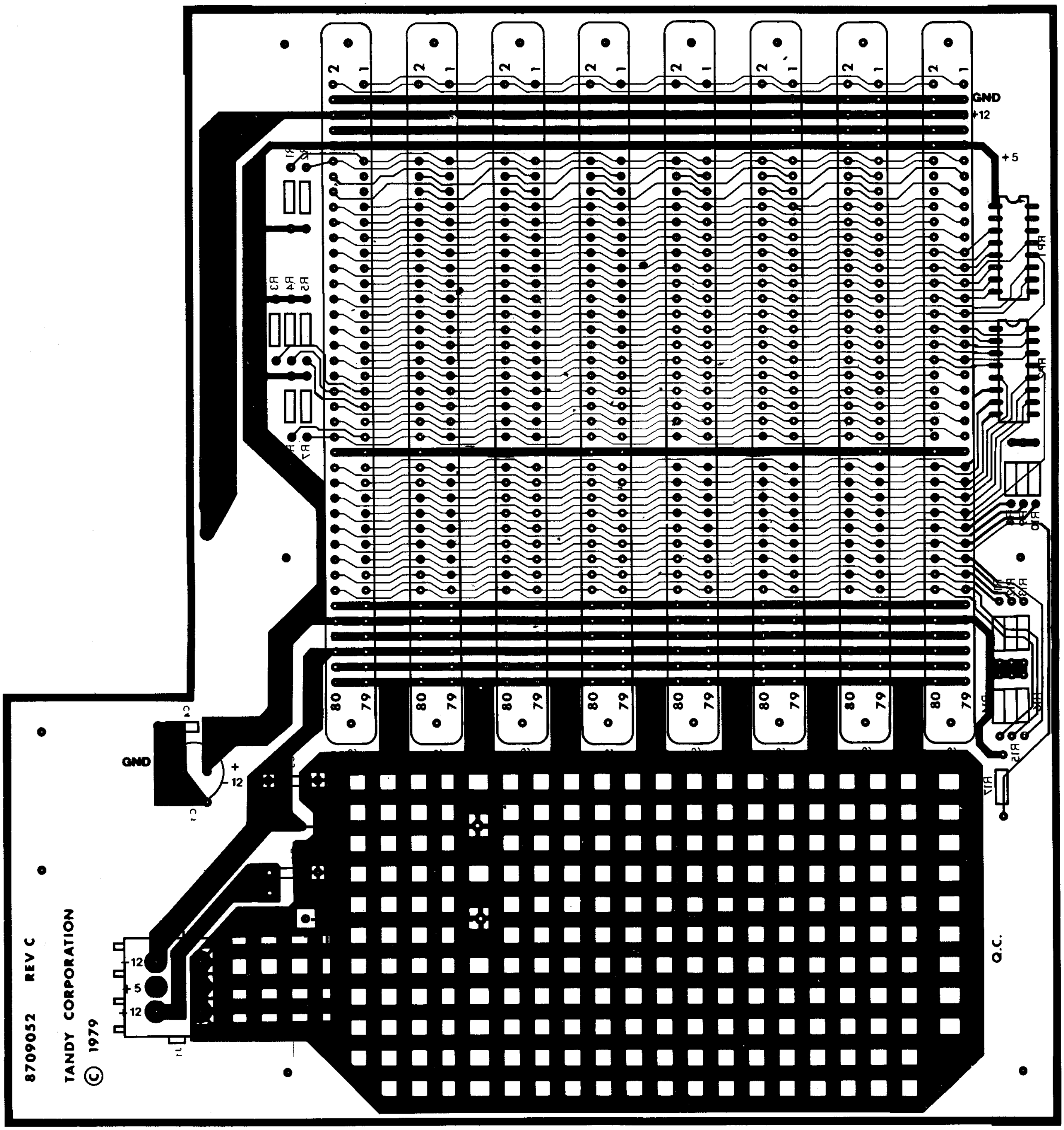


Figure 2. X-Ray View of Motherboard Printed Circuit Board — Circuit Side

SECTION XI

KEYBOARD UNIT

A. INTRODUCTION

The keyboard of the TRS-80 Model II is a 76-key, low profile, capacitive keyboard that utilizes an 8021 microprocessor chip.

The microprocessor and its associated electronics scan the key matrix, convert switch closures to an 8-bit digital code and then transmits that code serially to the keyboard interface on the Video/Keyboard Card.

The keyboard map (Figure 3) presents the actual code that TRSDOS will return to the user for each key on the keyboard, in each of the four modes — unshift, shift, caps and control.

The keyboard is connected to the main console by a built-in cable to an external cable from the bottom front of the console (see Figures 1 and 2).

Figure 1 shows the internal connections from the keyboard PC Board to the female DIN connector in the keyboard case.

Figure 2 shows the external connection from the DIN connector to the Video/Keyboard PC Board in the Video Display Console.

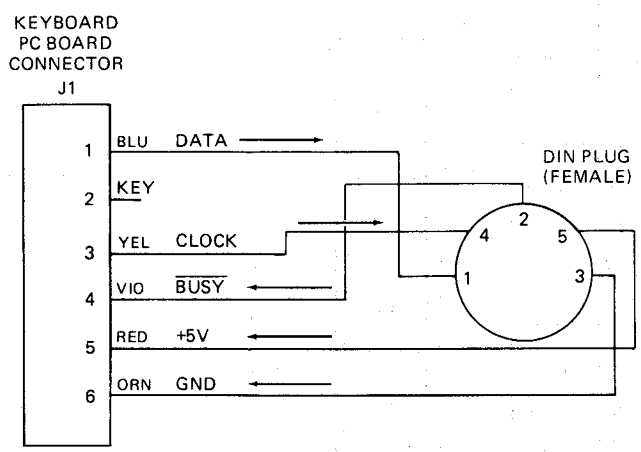


Figure 1. Keyboard Internal Cable

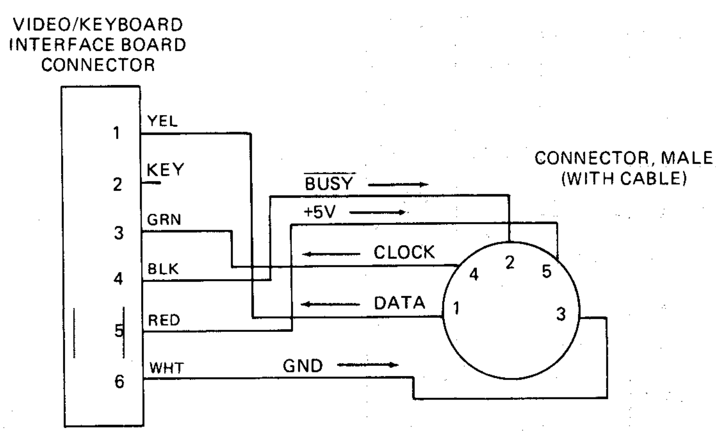


Figure 2. Keyboard External Cable

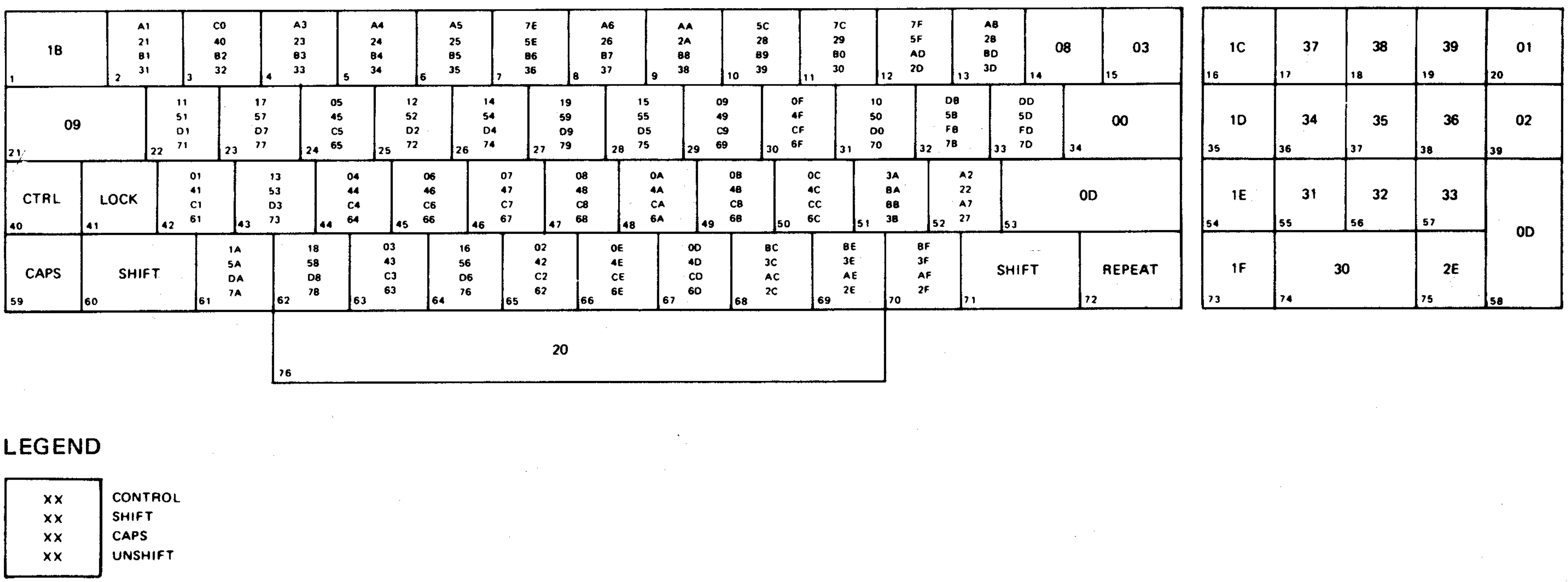


Figure 3. Keyboard Code Map

TRS-80 MODEL II KEYBOARD PARTS LIST

SYMBOL	DESCRIPTION	MANUFACTURER'S PART NUMBER	RADIO SHACK PART NUMBER
		CAPACITORS	
C1	10μF, 10V, Tantalum	————	ACC106QCTA
C2	0.033μF, 25V, Ceramic Disc	————	ACC333QFCP
C3	10μF, 10V, Tantalum	————	ACC106QTCA
C4	0.033μF, 25V, Ceramic Disc	————	ACC333QFCP
C5	0.033μF, 25V, Ceramic Disc	————	ACC333QFCP
C6	0.033μF, 25V, Ceramic Disc	————	ACC333QFCP
		CONNECTOR	
J1	6-pin, Right Angle	3900444000	AJ-6818
		DIODES	
CR1	LED, MV57152	2157152000	AL-1129
CR2	LED, MV57152	2157152000	AL-1129
		INTEGRATED CIRCUITS	
Z1	74366, Tri-State Hex Buffer	2274366001	AMX-4342
Z2	00950	2200950000	AMX-4341
Z3	00908	2200908003	AMX-4340
Z4	65-1991, Mask Rom, MUP	2008021013	AMX-4339
		KEYCAPS	
	ESC	BBWW25P1E3890701	AK-3972
	!/1	GKBB01P137010801	AK-3973
	@/2	GKBB01P137220801	AK-3974
	#/3	GKBB01P137030801	AK-3975
	$/4	GKBB01P137040801	AK-3976
	%/5	GKBB01P137050801	AK-3977
	/6	GKBB01P136160801	AK-3978
	&/7	GKBB01P137270801	AK-3879
	*/8	GKBB01P137180801	AK-3880
	(/9	GKBB01P137380801	AK-3981
	)/Ø	GKBB01P137900801	AK-3982
	-̲	GKBB01P110520802	AK-3983
	+/=	GKBB01P111270802	AK-3984
	BACK SPACE	BBWW01P1B3211101	AK-3985
	BREAK	BBWW01P1B3310701	AK-3986
	(left arrow)	BBWW01P110180101	AK-3987
	7	GKBB01P110070101	AK-3988
	8	GKBB01P110080101	AK-3989
	9	GKBB01P110090101	AK-3990
	F1	BBWW01P1F4010701	AK-3991
	TAB	BBWW45P1T5990701	AK-3992
	Q	GKBB01P1Q0010101	AK-3993
	W	GKBB01P1W0010101	AK-3994
	E	GKBB01P1E0010101	AK-3995
	R	GKBB01P1R0010101	AK-3996
	T	GKBB01P1T0010101	AK-3997
	Y	GKBB01P1Y0010101	AK-3998

TRS-80 MODEL II KEYBOARD PARTS LIST (Cont'd)

SYMBOL	DESCRIPTION	MANUFACTURER'S PART NUMBER	RADIO SHACK PART NUMBER
	KEYCAPS		
	U	GKBB01P1U0010101	AK-3999
	I	GKBB01P1I0010101	AK-4000
	O	GKBB01P1O0010101	AK-4001
	P	GKBB01P1P0010101	AK-4002
	[/	GKBB01P111240802	AK-4003
	]/	GKBB01P111250810	AK-4004
	HOLD	BBWW02P144670701	AK-4005
	(right arrow)	BBWW01P110170101	AK-4006
	4	GKBB01P110040101	AK-4007
	5	GKBB01P110050101	AK-4008
	6	GKBB01P110060101	AK-4009
	F2	BBWW01P1F4020701	AK-4010
	CTRL	BBWW01P1C3560701	AK-4011
	LOCK	BBZT92P1L4812062	AK-4012
	A	GKBB01P1A0010101	AK-4013
	S	GKBB01P1S0010101	AK-4014
	D	GKBB01P1D0010101	AK-4015
	F	GKBB01P1F0010101	AK-4016
	G	GKBB01P1G0010101	AK-4017
	H	GKBB01P1H0010101	AK-4018
	J	GKBB01P1J0010101	AK-4019
	K	GKBB01P1K0010101	AK-4020
	L	GKBB01P1L0010101	AK-4021
	:/;	GKBB01P111290802	AK-4022
	/	GKBB01P111300802	AK4023
	ENTER	BBWW46P1E3960701	AK-4024
	(up arrow)	BBWW01P110190101	AK-4025
	1	GKBB01P110010101	AK-4026
	2	GKBB01P110020101	AK-4027
	3	GKBB01P110030101	AK-4028
	CAPS	BBZT92P1270C2062	AK-4029
	Z	GKBB01P1Z0010101	AK-4030
	X	GKBB01P1X0010101	AK-4031
	C	GKBB01P1C0010101	AK-4032
	V	GKBB01P1V0010101	AK-4033
	B	GKBB01P1B0010101	AK-4034
	N	GKBB01P1N0010101	AK-4035
	M	GKBB01P1M0010101	AK-4036
	/,	GKBB01P110340802	AK-4037
	/.	GKBB01P110350802	AK-4038
	?//	GKBB01P118560802	AK-4039
	SHIFT	BBWW02P1S5770701	AK-4040
	REPEAT	BBWW25P1R5490701	AK-4041
	(down arrow)	BBWW01P110200101	AK-4042
	Ø (zero)	GKBB05P110100101	AK-4043
	· (decimal point)	GKBB01P110220104	AK-4044
	ENTER	BBWW05P1E3962304	AK-4045
	Space Bar, low profile	4400104001	AK-3934

TRS-80 MODEL II KEYBOARD PARTS LIST (Cont'd)

SYMBOL	DESCRIPTION	MANUFACTURER'S PART NUMBER	RADIO SHACK PART NUMBER
		RESISTORS	
R1	82 ohm, ¼W, 5%	-------------	AN0122EEB
R2	82 ohm, ¼W, 5%	-------------	AN0122EEB
R3	499 ohm, ¼W, 1%	-------------	
R4	301 ohm, ¼W, 1%	-------------	
R5	3K, ¼W, 5%	-------------	
R6	10K, ¼W, 5%	-------------	
		SPRINGS	
---	1.5 oz. Yellow, Low Profile	4500021015	ARB-6733
---	2.0 oz. Red, Low Profile	450002120	ARB-6734
---	1.5 oz. Yellow Low Profile	4500024015	ARB-6735
		SWITCHES	
---	Cap Standard, Low Profile	-------------	AS-0687
---	Target Light, Low Profile	-------------	AS-0688
		MISCELLANEOUS	
	Cable Harness, Keyboard, Internal	8893011	AW-2438
	Case, Lower	8719031	AZ-5198
	Case, Upper	8719032	AZ-5199
	DIN Plug, Connector, Female	8519020	AJ-6768
	Diskette, 8" TRSDOS (64K/32K)	8792027	AXX-2003
	Disk Terminator	8893527	AJ-6800
	Foot, Rubber (4)	8589005	AHB-7614
	Leg, Space Bar, Low Profile	4400103000	AF-0281
	Operator's Manual	8893515	AUM0063
	Power Cord, 8'	8709057	AW-2425
	Screw, 6-19 x 3/4" (19.05 mm) (6)	8569029	AHD-1538
	Screw, SFT, 3-28 x 3/8" (9.5 mm) (2)	4700192000	AHD-1571
	Mount, Space Bar, Low Profile	4400102000	ART-2775
	Cable Harness, Keyboard, External	8893919	AW-2437
	Connector, Male, with Cable	8519036	AJ-6782

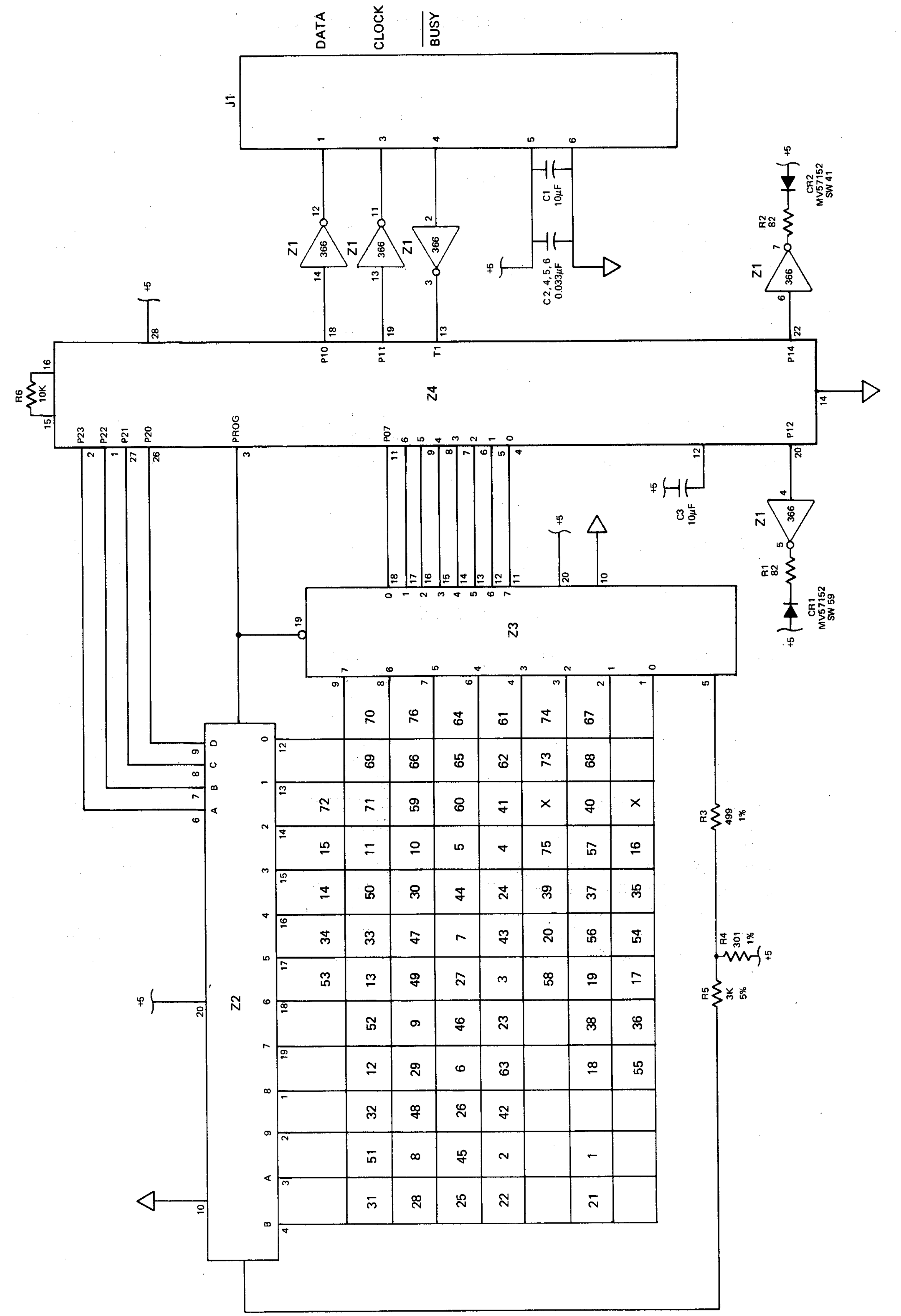


Figure 4. Keyboard Schematic Diagram

SECTION XII

PERIPHERAL INTERFACES

A. SERIAL INTERFACE CONNECTIONS

Two serial I/O channels are provided for connection to equipment such as telephone interface modems, serial line printers, etc. Channel A is designed to allow asynchronous or synchronous transmission. Channel B is designed for asynchronous transmission only.

Connections are made via two DB-25 connectors which conform to the RS-232-C standard. Pin-outs and signals available are listed below.

CHANNEL A

STANDARD RS-232-C SIGNAL	(PIN #)
I/O TRANSMIT S.E.T.	15
GROUND	1,7
RECEIVED DATA	3
RECEIVER CLOCK	17
TRANSMIT CLOCK	24
DATA SET READY	6
CLEAR-TO-SEND	5
CARRIER DETECT	8
TRANSMIT DATA	2
REQUEST-TO-END	4
DATA TERMINAL READY	20

CHANNEL B

STANDARD RS-232-C SIGNAL	PIN #
GROUND	1,7
RECEIVED DATA	3
RECEIVER XMITTER CLOCK	17
DATA SET READY	6
CLEAR-TO-SEND	5
CARRIER DETECT	8
TRANSMIT DATA	2
REQUEST-TO-SEND	4
DATA TERMINAL READY	20

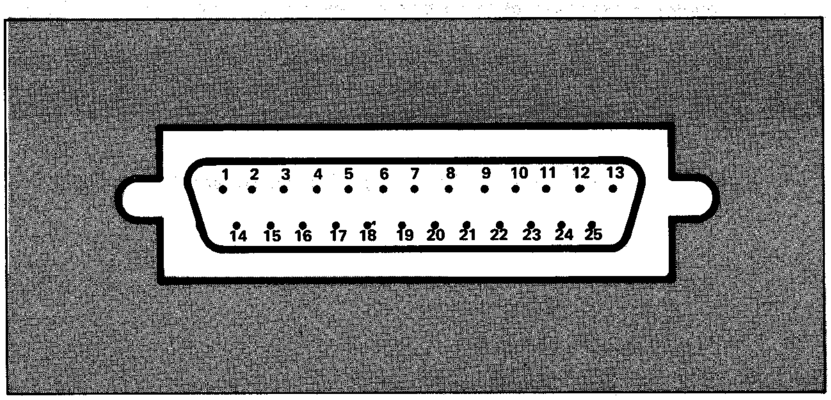


Figure 1. Serial Interface Connector (DB-25)

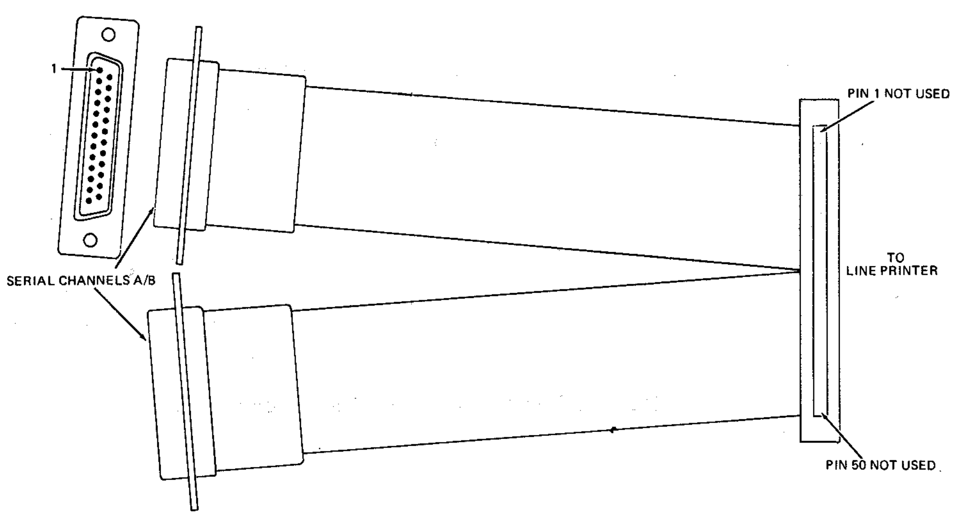


Figure 2. 50-Conductor Ribbon Cable (split 25/25)

B. PARALLEL INTERFACE

The Model II provides one parallel I/O channel for connection to a line printer via the 34-pin connector on the back panel of the Display Console. Eight data bits are output in parallel and four data bits are input. All levels are TTL compatible.

Connector pin-outs and available signals are listed on the following page.

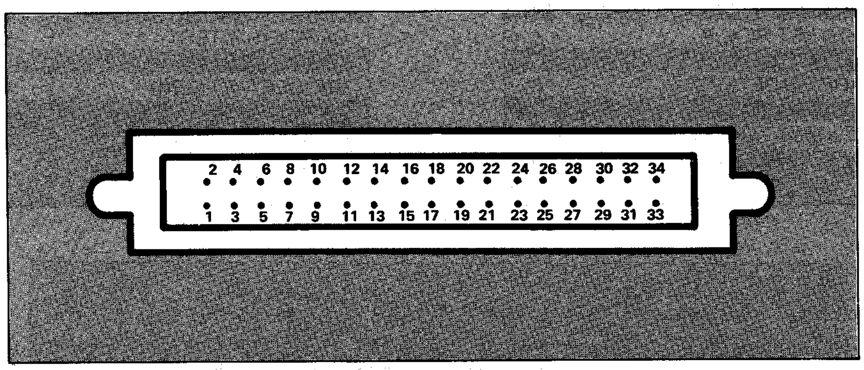


Figure 3. Parallel Interface 34-pin Connector

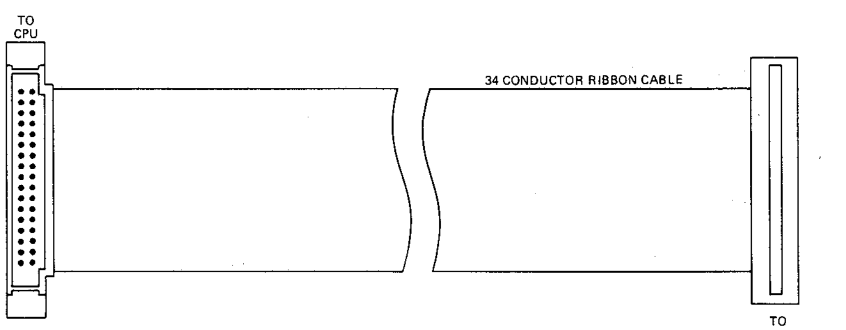


Figure 4. Parallel Interface 34-pin Ribbon Cable

PARALLEL INTERFACE – SIGNAL DESCRIPTIONS

SIGNAL	FUNCTION	PIN#
STROBE*	1 μS pulse to clock the data from processor to printer	1
DATA 0	Bit 0 (lsb) of output data byte	3
DATA 1	Bit 1 of output data byte	5
DATA 2	Bit 2 of output data byte	7
DATA 3	Bit 3 of output data byte	9
DATA 4	Bit 4 of output data byte	11
DATA 5	Bit 5 of output data byte	13
DATA 6	Bit 6 of output data byte	15
DATA 7	Bit 7 (msb) of output data byte	17
ACK*	Input to Computer from Printer, low indicates data byte received	19
BUSY	Input to Computer from Printer, high indicates busy	21
PAPER EMPTY	Input to Computer from Printer, high indicates no paper – if Printer doesn't provide this, signal is forced low	23
SELECT	Input to Computer to Printer, high indicates device selected	25
PRIME*	Output to Printer to clear buffer and reset printer logic	26
FAULT*	Input to Computer from Printer low indicates fault (paper empty, light detect, deselect, etc.)	28
GROUND	Common signal ground	2,4,6,8,10 12,14,16,18, 20,22,24,27, 31,33
NC	Not connected	29,30,32,34

*These signals are active low.

C. DISK EXPANSION CONNECTOR

A floppy disk I/O channel is provided for connection of the Model II Disk Expansion Unit.

NOTE: When the disk expansion unit is not connected to the Model II, a special terminator must be connected to the Disk Expansion connector on the back of the Display Console.

The terminator is a PC Board which provides jumpering to the termination resistors on the Computer's FDC board. When using the computer in conjunction with a disk expansion unit the terminator is removed and termination is then provided on drive #1 in the expansion unit.

Connector pin-outs and signal descriptions are listed in the Floppy Disk Controller section of this service manual.

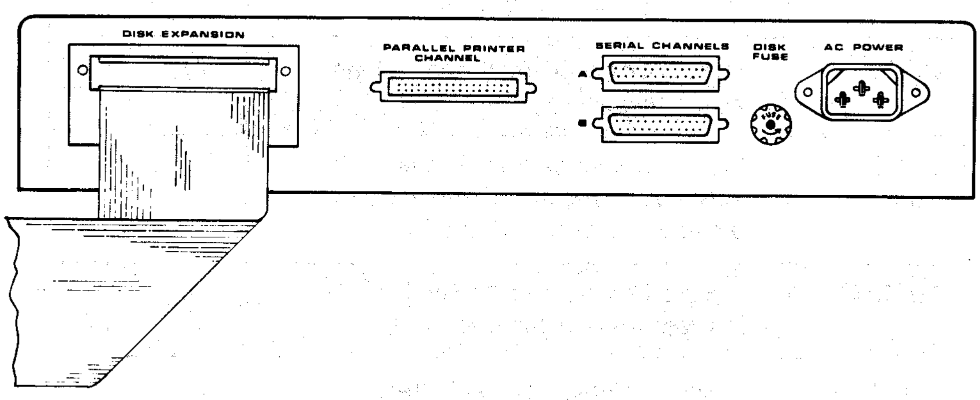


Figure 5. Rear View of the TRS-80 Model II Microcomputer

SECTION XIII

DISK EXPANSION UNIT

A. INTRODUCTION

The TRS-80 Model II Disk Expansion Unit is a mass storage device designed to interface with the TRS-80 Model II Computer to provide the user with an additional storage capacity of up to 1.5 Megabytes for a total system capacity of 2 Megabytes on line.

The Disk Expansion Unit is available in a 1, 2, or 3 drive configuration. The 1 and 2 drive units may be upgraded with additional drives from your Radio Shack dealer.

The Disk Expansion Unit consists of up to three flexible disk drives, a power supply and a cooling fan. It connects to the Computer through a flat ribbon cable.

Standard 115/120 VAC is applied to the expansion unit through a power switch where it is distributed to the three disk drives, the internal power supply and to its cooling fan.

The power supply converts the AC input to three levels of DC which is routed to the disk drives for their logic signals. The DC voltages are +24, +5 and −12. A LED on the fron panel "lights up" when the power switch is in the "ON" position.

Subassembly Description

The disk expansion unit consists of seven major subassemblies. Each subassembly may be considered as a single component of the disk expansion system. If a subassembly is determined to be faulty, the entire subassembly should be replaced.

1. **Chassis:**

   The Chassis assembly consists of a metal chassis which forms the bottom and back panel of the unit. Also included in the chassis assembly are the line cord and three fuse holders. The bottom of the chassis has two raised supports for attaching the disk drive mounting brackets.

2. **Power Supply:**

   The power supply assembly is a 60 watt, switching power supply which provides the following voltages to the disk drives:

+5 Volts DC	@	3.00 Amps
-12 Volts DC	@	0.17 Amps
+24 Volts DC	@	1.70 Amps

NOTE: The −12 volt output is not used.

The power Supply is regulated and has overcurrent protection. It will operate at either 50Hz or 60Hz input and may be jumpered for either 95VAC to 135VAC or 190VAC to 270VAC. The Power Supply is located in the rear and to the left of the CRT.

3. **Disk Drive:**

   The disk drive is an 8" flexible disk unit capable of supporting both single and double density recording formats. All of the disk drive control signals come from the Floppy Disk Controller PC board in the computer. The drive contains two motors; one is an AC motor which rotates the diskette at constant speed, the other motor is a DC stepping motor which positions the read/write head over one of 77 tracks on the diskette. The electronics on the disk drive control the stepping motor and convert the signals from and to the read/write head into correct format.

   NOTE: Models for overseas shipment may be configured with an AC Motor for the line voltage available in that country and may be fitted with a different drive pulley for 50 Hz line frequency.

4. **Wiring Harness:**

   All internal wiring of the disk expansion unit is accomplished with one wiring harness assembly. It includes both AC and DC wiring for the system as well as providing proper grounding.

5. **Fan:**

   Cooling for the system is provided by a single rotary fan which is mounted in the bottom of the chassis assembly and is protected by a finger guard on the outside of the chassis.

6. **Bezel:**

   The bezel assembly consists of the plastic front bezel, the AC power switch, power indicator LED, and blank hole cover for unused drive positions. It is mounted to the top cover with seven plastite screws.

7. **Top Cover:**

   The top cover is a formed sheet metal cover with air slots for cooling. It mounts with thread forming screws in the back and on both sides.

B. SWITCH CONFIGURATIONS

9404A (Discreet Logic) CDC Drives

1. PC Board #75890770. See **CDC Hardware Maintenance Manual**, page 9, Figure 5-3A.
   a) S1-5 – "ON" Position
   b) Drive #1 – S1-2 – "ON" Position
      Drive #2 – S1-3 – "ON" Position
      Drive #3 – S1-4 – "ON" Position
   c) All other positions on S1 should be "OFF".

2. PC Board #75881970. See **CDC Hardware Maintenance Manual**, page 10, Figure 5-3A.
   a) S1-5 – S1-2 – "ON" Position
   b) Drive #1 – S1-2 – "ON" Position
      Drive #2 – S1-3 – "ON" Position
      Drive #3 – S1-4 – "ON" Position
   c) All other positions of S1 – "OFF" Positon.
   d) S3-4 – "ON" Position
   e) All other positions of S3 – "OFF" Position.

9404B (LSI Logic) CDC Drives

1. PC Board #77643120. See **CDC Hardware Maintenance Manual**, page 12, Figure 5-3B.
   a) Drive #1 – S1-2 – "ON" Position
      Drive #2 – S1-3 – "ON" Position
      Drive #3 – S1-4 – "ON" Position

Drive #1 Only, All Boards (Discreet and LSI)

1. DIP Terminator Pak installed in "RMI" (see Board diagrams, section 5-3, **CDC Hardware Maintenance Manual**).

C. TEST POINTS

All CDC Drives:

Refer to the **CDC Maintenance Manual** and to Figure 1 on the following page.

1. Figure 1 shows suggested locations to be used as test points. The arrows point to a component lead or plate through hole that may be used for the corresponding signals.

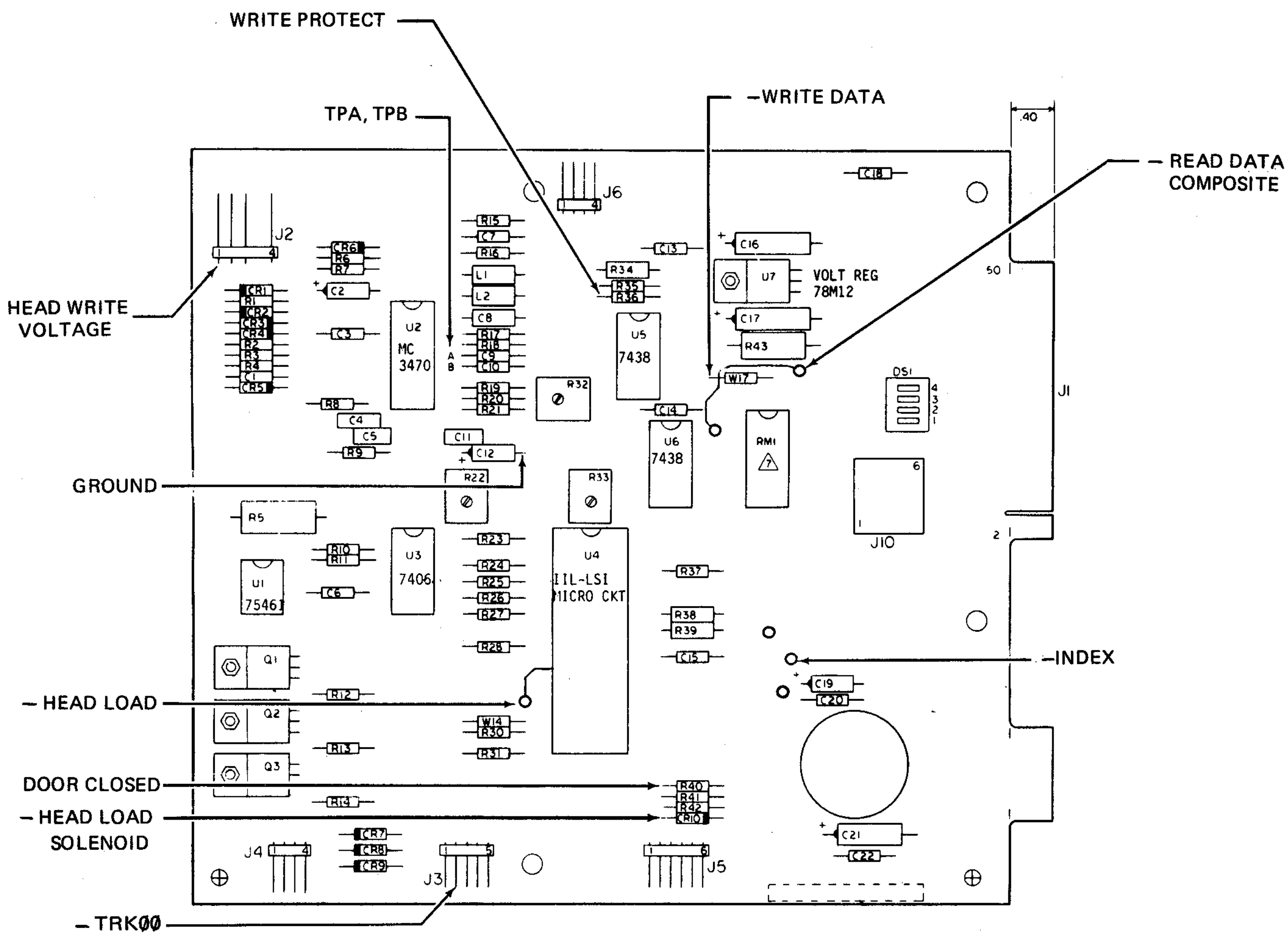


Figure 1. CDC Model 9404B PCB Test Points and Component Locations.

Signal	Description
TPA	Head Amplitude
TPB	Head Alignment
–HEAD LOAD	–HEAD LOAD signal from the computer. Head is loaded when low.
–HEAD LOAD SOLENOID	Low logic signal – activates the Head Load Solenoid.
–INDEX	Indicates the index hole has been detected by the FDC. Used for scope synchronization. Check for INDEX detection.
–WRITE DATA	Serial data from the FDC to drive logic. TTL logic level signal.
HEAD WRITE VOLTAGE	Analog waveform test point. Assures integrity of the write logic circuitry.
–READ DATA COMPOSITE	Unseparated data and clock information supplied to the FDC from drive logic. TTL level signal.
WRITE PROTECT	This signal should be high when a write protected diskette (diskette write protect slot uncovered) is fully inserted in drive.
–TRKØØ	–TRKØØ should be low when the track ØØ switch is closed.
DOOR CLOSED	Signal high reflects door closed status to the drive logic.

SECTION XIV

TROUBLESHOOTING - DISK SYSTEM

A. TROUBLESHOOTING PROCEDURE

This section of the manual will guide service personnel through a subassembly check-out procedure which should locate a faulty subassembly. That subassembly may then be removed and replaced.

AC or DC Power Failures:

1. Remove Cover/Bezel Assembly (see System Disassembly in Section B. Replacement Procedures).

2. Plug the power cord into an AC outlet and turn the power switch on (front bezel). Check for the following:

   a) Fan is running, AC spindle Motor on disk drive is running, and power LED is lit.

   b) In case of failure: If none of these conditions are met, then check the AC input terminals to the power supply with a voltmeter. If no voltage is measured here then check for voltage at the power switch. No voltage at the power switch indicates a faulty power cord.

   c) If fan isn't running, check that fan cord is plugged securely on fan terminals. Check for AC at fan cord plug and trace backwards with a voltmeter to terminal block (TB2) if no voltage is found. (See Wiring Diagram, Figure 1.)

   d) If disk drive motor isn't running, check the fuse for that unit on the back of the chassis. Next trace the wiring back to TB2 with a voltmeter.

   e) If fuse continues to blow, check for a short on TB2. Next disconnect AC plugs on disk drives and check harness for shorts. Next, reconnect AC plugs to drives one by one until unit causing failure is found. Replace the faulty disk drive.

   f) If LED does not light, it indicates either a bad LED or a +5 volt circuit failure. First, check all DC voltages (+5V $\pm$2%; -12V $\pm$5%; +12V $\pm$10%) at the power supply output terminals (see Figure 1). If the correct voltages are not present then disconnect the wiring harness from the output terminals, install a 4 ohm, 5 watt resistor between +5 and COM and check voltages again.

   NOTE: The +24 volt terminal will usually read high under this condition (up to 30 volts). Incorrect voltage readings at this point indicate a faulty power supply. If voltage readings are OK with the dummy load, then an overcurrent condition in the system is indicated. Check for shorted LED circuit. Reconnect wiring harness to power supply and disconnect DC plugs to disk drives (see schematic). If power supply still fails then a faulty wiring harness or short on TB1 is indicated. If LED is lit then reinstall DC plugs on drives one by one until unit causing failure is found. A disk drive causing the power supply to fail should be replaced.

Operational Failures:

1. Check for the correct switch position on the CDC drive PC Board (see **B. Switch Configurations** in the **Disk Expansion Unit** section).

2. Install the Diagnostic Diskette in drive Ø and refer to the Troubleshooting Manual. This test will exercise all disk drives in the system by doing seeks, reads and writes.

Read or Write Error:

First, replace the **System** diskette in the failing drive with a known good Media. Next, check the jumpers on all drives. Then, check voltages on the DC connector to the failing drive. Now, replace the signal cable with a known good cable. If the failure persists, then replace the drive.

NOTE: A failure may appear on any drive because of incorrect termination on drive 1. Be sure termination resistor pack (on CDC drive) or jumper plugs (on Shugart drive in Computer) are correctly installed on drive 1. See **B. Switch Configurations** in the **Disk Expansion Unit** section for the CDC drive and **B. Jumper Configuration** in the **Floppy Disk Drive** section for the Computer disk drive.

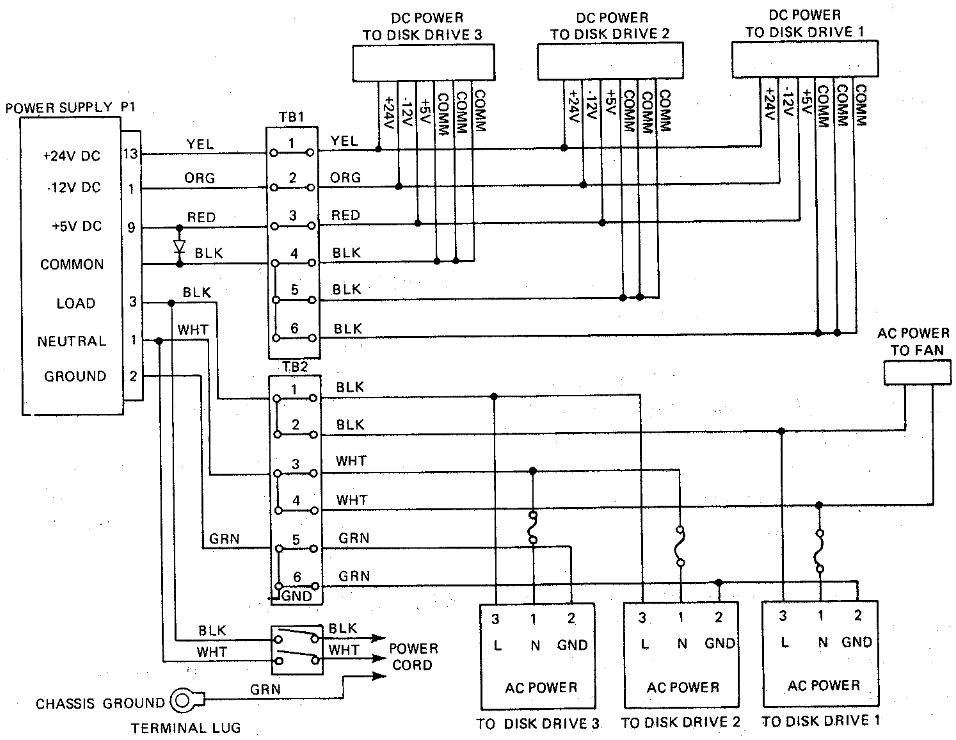


Figure 1. Disk Expansion Unit Wiring Diagram

B. REPLACEMENT PROCEDURES

NOTE: Be sure that the power cord is unplugged while any assembly or disassembly is in progress.

System Disassembly

1. Cover & Bezel Assembly

a) Remove four screws from each side of cover and seven screws from rear edges of chassis.
b) Slide the cover/bezel assembly forward about 1 inch then tilt the rear of the cover up so that the bezel lays face down in front of the chassis. **NOTE:** Be careful that the cover doesn't hang on the signal cable or wiring harness when lifting it. The length of the wiring harness to the bezel does not permit any other procedure for removing the cover/bezel assembly.

2. Power Supply

a) Remove Cover/Bezel Assembly.
b) Disconnect all AC, DC, and ground terminals from power supply.
c) Remove four Mounting Screws from back of chassis.
d) Remove power supply.

3. Disk Drive

NOTE: When replacing a CDC 9404A drive with a 9404B drive, the DC adapter cable must be disconnected from the end of the harness in order to plug the DC connector onto J10 on the drive. If the drive being replaced is in the Drive #1 position, then the DC adapter must be replaced with the 9404B DC adapter and plugged into J7 (card edge connector) on the drive. The 9404B DC adapter is available from National Parts as no. AW2460. The 9404B drive may be identified by a 40-pin LSI chip near the center of the PC Board on the drive.

a) Remove Cover/Bezel Assembly.
b) Disconnect Signal Cable from drive.
c) Disconnect AC and DC connectors from drive.
d) Turn complete expansion unit on its side and remove the two disk drive mounting screws (front and rear). These screws are accessible through holes in the bottom of the chassis. Support the drive so it doesn't fall out of the assembly when mounting screws are removed.

4. Fan

a) Remove Cover/Bezel Assembly.
b) Turn expansion unit on its side and remove the four Fan mounting screws and the finger guard. **NOTE:** Be careful to retrieve all nuts and washers inside chassis to prevent possible shorting.
c) Turn chassis back to its normal position and lift fan so that the cable may be unplugged.
d) Remove Fan.

5. Wiring Harness

a) Remove Cover/Bezel Assembly.
b) Disconnect AC and DC Connectors from drives.
c) Disconnect plug-on terminals from fuse holders.
d) Remove two mounting screws for power switch on the bezel. The power cord must be disconnected from switch.
e) Slit shrink tubing on LED leads and disconnect push-on terminals from LED. Note polarity.
f) Remove two mounting screws for each of the terminal blocks.
g) Note the location of all tie wraps then cut them loose.
h) Remove wiring harness.

6. Signal Cable

a) Remove Cover/Bezel Assembly.
b) Remove top screw from cable clamp on the rear of the chassis and loosen the bottom screw.
c) Disconnect signal cable from disk drives.
d) Remove signal cable.

7. Power Cord

a) Remove Cover/Bezel Assembly.
b) Disconnect Black & White power cord wires from switch on bezel and the green wire from chassis. **NOTE:** Some models require desoldering.
c) Snap strain relief out of hole in rear of chassis. **NOTE:** A screwdriver may be used on the inside of one side of the strain relief then the other side to pop it out of the hole.

8. LED

a) Remove Cover/Bezel Assembly
b) Slit shrink tubing and remove the push-on terminal from the LED
c) Press the LED out of its socket from the front. **NOTE:** The eraser end of a pencil works well for this.

Subassembly Replacement

1. **Cover/Bezel Assembly**

   NOTE: The cover and the bezel may be purchased separately (see Parts List). The bezel mounts to the cover with seven plastite screws from the inside.

   a) Be sure that the power switch wires are not shorting and that the LED polarity is correct. Also check the routing of all harness wires, especially along the right hand side where the cover mounting screws could interfere.
   b) Tilt the cover/bezel assembly down over the chassis. Be careful not to snag any cables. Slide toward the rear of the chassis.
   c) Insert two screws in the top rear corners of the chassis but do not tighten. **NOTE**: Be sure that the bezel is properly centered around the disk drives.
   d) Insert two screws in the bottom rear corners of the chassis. Snug the four rear screws.
   e) Insert four screws in each side of the cover. **NOTE**: The chassis may sag in the middle, in which case the chassis should be supported in the middle. An extra foot is handy for this. An awl may be used to help line up the holes.
   f) Insert the remaining screws in the rear and tighten all screws.

2. **Power Supply**

   a) Follow disassembly procedure in reverse.
   b) **The Disk Wiring Diagram, Figure 1, may be used for correct hookup of the harness to the power supply.**

3. **Disk Drive**

   a) Follow the disassembly procedures in reverse. **NOTE**: Due to possible warp in the chassis, it may be necessary to loosen the screws that secure the disk drive mounting bracket to the chassis. These screws may be reached with a long handled screwdriver between the disk drives.
   b) Be sure that all wiring is routed away from both of the disk drive motors and the stepping motor shaft.

4. **Fan**

   a) Follow disassembly procedure in reverse. **NOTE**: Be sure that the plug is pushed securely onto the fan terminals. Also, see that the large harness of wires running in front of the fan is below the bottom of the #2 disk drive.
   b) Route all wires for best air flow while keeping them away from drive motors.

5. **Wiring Harness**

   a) Follow disassembly procedure in reverse. **NOTE**: Tie wraps should be reinstalled where they were before and as needed.

6. **Signal Cable**

   a) Follow disassembly procedure in reverse. **NOTE**: Be sure the cable is centered in the cable clamp before tightening it.
   b) Be sure the signal cable is bowed away from the disk drives between connectors.

7. **Power Cord**

   a) Insert cord through hole in right rear of chassis.
   b) Connect the black and white wires to the power switch and the green wire directly to the metal chassis next to TB1.
   c) Leave a little slack in the cord with the bezel laying face down in front of the chassis and install the strain relief in the chassis hole.

8. **LED**

   a) Press the LED into its mounting socket from the rear. It will snap into place. **NOTE**: A phillips head screwdriver is handy for this.
   b) Slip a piece of shrink tubing on each of the LED wires and connect the push-on terminals to the LED
   c) Turn power on to check for correct polarity. If LED doesn't light, reverse leads.
   d) Slip shrink tubing down to where it contacts the LED body and heat the tubing to complete the installation.

DISK EXPANSION UNIT MECHANICAL PARTS LIST

DESCRIPTION	MANUFACTURER'S PART NUMBER	RADIO SHACK PART NUMBER
	BRACKETS	
Mounting *(2), †(4), ◇(6)	8729027	ART2688
Mounting, PCB *(1), †(2), ◇(3)	8729030	AHB9448
	CABLES	
Disk Assembly	8709091	AW2427
Disk II Wiring Harness	8893013	AW2439
Power, fan	8709079	AW2426
Power Supply Harness	8893512	
Signal Subassembly	8893455	AW2455
	CASE	
Bezel	8719049	AZ5200
Bumper, molded (4)	8719054	AHB9441
Chassis, flat black	8729020	AZ5227
Cover, flat black *(2), †(1)	8729025	AZ5228
Cover, silver	8729019	AZ5226
	NUTS	
Hex, #4 (4)	8579001	AHD7165
Hex, #6 *(6), †(8), ◇(10)	8579014	AHD7168
	SCREWS	
4 x 1/2" (12.7mm), machine (8)	8569033	AHD1542
6 x 3/8" (9.5mm), machine *(4), †(8), ◇(12)	8569003	AHD1355
6 x 3/8" (9.5mm), Plastite *(7), †(5), ◇(3)	8569047	AHD1552
6 x 3/8" (9.5mm), thread-forming (17)	8569042	AHD1549
6 x 2" (50.8mm), slot, hex (4)	8569052	AHD8499
8 x 3/8" (9.5mm), thread-forming *(9), †(13), ◇(17)	8569030	AHD1539
10 x 1/4" (6.35mm), machine *(1), †(2), ◇(3)	8569044	AHD1551
10 x 3/8" (9.5mm), machine *(2), †(4), ◇(6)	8569043	AHD1550
	SWITCH	
Rocker, 4A	8489017	AS9126
	WASHERS	
1/4" (6.35mm) (8)	8589015	AHD8512
#4, lock (4)	8589021	AHD8518
#6, flat *(8), †(12), ◇(16)	8589017	AHD8514
#6, lock *(8), †(12), ◇(16)	8589018	AHD8515
#8, flat *(9), †(13), ◇(17)	8589016	AHD8513
#8, lock *(5), †(9), ◇(13)	8589013	AHD8511
#10, lock *(3), †(6), ◇(9)	8589020	AHD8517

*Quantity for Disk Expansion Unit with1 drive.
†Quantity for Disk Expansion Unit with 2 drives.
◇Quantity for Disk Expansion Unit with 3 drives.

DISK EXPANSION UNIT MECHANICAL PARTS LIST (cont'd)

DESCRIPTION	MANUFACTURER'S PART NUMBER	RADIO SHACK PART NUMBER
	MISCELLANOUS	
Adapter Assembly *(1), †(2), ◊(3)	8893007	AW2454
Cord, power	8709057	AW2454
Fan	8790505	AXX5008
Finger Guard	8729002	ART2676
Fuse, 2A (3)	8479001	AHF1160
Fuse Holder w/hardware (3)	8519048	AHF1161
Insulator, paddle board *(1), †(2), ◊(3)	8709080	AHB9437
LED, red	8469004	AL1102
LED Mounting	8559001	ART1951
Power Supply, AA11100	8790017	AXX6002
Strain Relief	8719053	AHB9440
Support, zinc plated	8729023	ART2687
Terminal Ring (2)	8539004	AHB9416
Tubing, clamp-less (2)	8729022	AHB9445

*Quantity for Disk Expansion Unit with 1 drive.

†Quantity for Disk Expansion Unit with 2 drives.

◊Quantity for Disk Expansion Unit with 3 drives.

9404B DISK DRIVE MECHANICAL PARTS LIST

To find the Radio Shack Part Number for mechanical parts to the Disk Drive, find the required part using the illustrations and parts lists beginning on page 8-1 of the **Control Data Maintenance Manual** located in the back of this Technical Reference Manual. Using the appropriate part's name and reference number, locate that part in the following list.

REF. NUMBER	DESCRIPTION	RADIO SHACK PART NUMBER
138	Actuator Assembly	ART2353
369	Arm, Disk Load	ART2339
175	Bail Armature	ART2333
292	Bar, Torsion, Door	ART2360
290	Bearing, Ball, Ext. Inner R	ART2351
321	Bearing, Cylindrical	ART2342
289	Bearing, Flanged	ART2336
362	Bearing, Spacer	ART2347
180	Belt, Flat	AB7043
144	Bracket, Connector	ART2361
304	Bracket, Latch	ART2356
207	Bumper, Door	ART2328
172	Bushing	ART2335
302	Bushing, Door Inject	ART2359
322	Bushing, Pushrod Molded	ART2340
323	Bushing, Pushrod Molded	ART2341
142	Cable, Lower Harness Assembly	AW2378
318	Carriage Assembly	ART2352
358	Carriage Head Assembly	AH4382
218	Carriage Stop	ART2326
177	Carriage Stop Kit	ART2350
365	Clamp, Stepper Motor	ART2346
184	Clip, Push-in	ART2329
183	Clip, Push-in	ART2330
171	Cone Assembly	ART2337
312	Cone, Disk Load	ART2324
252	Connector Housing	ART2354
287	Door, Black	ADA0277
311	Expander Cone	ART2325
174	Extension Armature	ART2334
179	Foam Pad	ART2331
366	Guide, Carriage	ART2345
267	Knob, Lever	AK3575
263	Latch, Door Inject Mold	ART2358
303	Lever, Door	ART2357
102	Motor Assembly, Drive	AM4509
280	Motor Assembly, Stepper	AM4508
260	Mount, Switch	ART2349
370	Pin, Disk Load Arm	ART2338
266	Pin, Grooved	AHB8952
210	Plate, Nut	ART2327
226	Pulley, Motor	ARA2732
363	Pulley, Spindle	ARA2731
176	Pushrod Assembly	ART2332
194	Retaining Ring	AHE0019
314	Retaining Ring	AHE0020

9404B DISK DRIVE MECHANCIAL PARTS LIST (cont'd)

REF. NUMBER	DESCRIPTION	RADIO SHACK PART NUMBER
310	Shaft, Disk Load	ART2362
173	Solenoid	AS9111
361	Spindle	ART2348
182	Spring, Compression	ARB6521
181	Spring, Compression	ARB6522
313	Spring, Cone	ARB6524
315	Spring, Garter	ARB6523
217	Spring, Leaf	ARB6525
368	Support, Assembled	ART2344
353	Switch, Actuator	AS0965
251	Switch, Optical	AS0968
261	Switch, Sub-mini	AS0966
147	Switch, Track	AS0967
248	Washer	AHD8448
189	Washer, Nylon	AHD8450
317	Washer, Special	AHD8447
316	Washer, Special	AHD8452
335	Washer, Special	AHD8453
178	Washer, Spring Lock	AHD8451
192	Washer, Spring Wave	AHD8449
291	Washer, Spring Wave	AHD8454
125	Write Protect Assembly	ART2355

9404B DISK DRIVE ELECTRICAL PARTS LIST

SYMBOL	DESCRIPTION	RADIO SHACK PART NUMBER
	CAPACITORS	
C1	47pF, 100V, monolithic	ACC476KLCP
C2	47pF, 100V, monolithic	ACC476KLCP
C3	47pF, 100V, monolithic	ACC476KLCP
C4	4.7µF, 6V, tantalum	ACC475MATP
C5	220pF, 100V, monolithic	ACC227KLCP
C6	0.10µF, 50V, monolithic	ACC104ZJCP
C7	0.10µF, 50V, monolithic	ACC104ZJCP
C8	4.7µF, 35V, tantalum	ACC475KGTP
C9	0.10µF, 50V, monolithic	ACC104ZJCP
C10	4.7µF, 6V, tantalum	ACC475MATP
C11	750pF, 100V, mica	ACC757GLWP
C12	330pF, 100V, mica	ACC337GLWP
C13	330pF, 100V, mica	ACC337GLWP
C14	0.10µF, 100V, monolithic	ACC100KLCP
C15	4.7µF, 35V, tantalum	ACC475KGTP
C16	0.10µF, 100V,	ACC104KLCP
C17	0.10µF, 50V, monolithic	ACC104ZJCP
C18	0.01µF, 100V, monolithic	ACC100KLCP
C19	0.01µF, 100V, monolithic	ACC100KLCP
C20	4.7µF, 10V, tantalum	ACC475MCTP
C21	0.1µF, 50V, monolithic	ACC104ZJCP
C22	0.01µF, 100V, monolithic	ACC100KLCP
C23	1µF, 25V,	ACC105ZFCP
C24	6.8µF, 35V, tantalum	ACC685MGTP
C25	6.8µF, 35V, tantalum	ACC685MGTP
C26	0.01µF, 100V, monolithic	ACC100KLCP
C27	4.7µF, 35V, tantalum	ACC104KLCP
C28	4.7µF, 35V, tantalum	ACC475MGTP
C29	0.10µF, 50V, monolithic	ACC104ZJCP
C30	0.1µF, 100V, monolithic	ACC104OLCP
C31	3.3µF, 35V,	
C32	1000µF, 100V, monolithic	ACC108KLCP
C33	47pF, 500V, mica	ACC476OUWP
C34	1000µF, 100V, monolithic	ACC108KLCP
C35	47pF, 100V, monolithic	ACC476KLCP
C36	120pF, 100V, monolithic	ACC127KLCP
C37	2.7µF, 6V, tantalum	ACC275KATP
C38	0.1µF, 50V, monolithic	ACC104ZJCP
C39	4.7µF, 6V, tantalum	ACC475MATP
C40	0.1µF, 50V, monolithic	ACC104ZJCP
C41	4.7µF, 35V, tantalum	ACC475MGTP
C42	Not Used	———
C43	15µF, 16V, tantalum	ACC156KATP
C44	Not Used	———
C45	33µF, 10V, tantalum	ACC336KCTP
C46	0.1µF, 50V, monolithic	ACC104ZJCP
C47	Not Used	———
↓	↓	↓
C51	Not Used	———
C52	0.1µF, 50V, monolithic	ACC104ZJCP
	CAPACITORS (cont'd)	
C53	Not Used	———
↓	↓	↓
C57	Not Used	———
C58	0.1µF, 50V, monolithic	ACC104ZJCP
C59	Not Used	———
↓	↓	↓
C63	Not Used	———
C64	0.10µF, 50V, monolithic	ACC104ZJCP
C65	Not Used	———
C66	Not Used	———
C67	Not Used	———
C68	0.01µF, 100V, monolithic	ACC100KLCP
C69	0.01µF, 100V, monolithic	ACC100KLCP
C70	Not Used	———
C71	0.1µF, 50V, monolithic	ACC104ZJCP
	COILS	
L1	22µh	———
L2	22µh	———
L3	100µh	———
L4	100µh	———
	DIODES	
CR1	1N914A	ADX1165
↓	↓	↓
CR9	1N914A	ADX1165
CR10	Not Used	———
CR11	1N4001	ADX1221
↓	↓	↓
CR15	1N4001	ADX1221
CR16	Not Used	———
CR17	1N914A	ADX1165
CR18	1N4820	ADX1291
CR19	1N4001	ADX1221
CR20	1N770	ADX1290
	INTEGRATED CIRCUITS	
U1	LM319	———
U2	733C	AMX4199
U3	733C	AMX4199
U4	78M12, voltage regulator	———
U5	75461	———
U6	7410, triple 3-input NAND	AMX3676
U7	7410, triple 3-input NAND	AMX3676
U8	7486, quad 2-input EXCLUSIVE-OR	AMX4317

9404B DISK DRIVE ELECTRICAL PARTS LIST (cont'd)

SYMBOL	DESCRIPTION	RADIO SHACK PART NUMBER
	INTEGRATED CIRCUITS (cont'd)	
U9	7474, Dual "D" flip-flop positive-edge-triggered	AMX3681
U10	LM319	———
U11	3086, dual transistor array	AMX4197
U12	7405, Hex inverter	AMS4315
U13	7400, quad 2-input NAND	———
U14	7438, qaud 2-input NAND buffer	AMX3683
U15	7438, quad 2-input NAND buffer	AMX3683
U16	9602, dual one-shot, re-triggerable	AMX3694
U17	9602, dual one-shot, re-triggerable	AMX3694
U18	7400, quad 2-input NAND	———
U19	7474, dual "D" flip-flop positive-edge-triggered	AMX3681
U20	7408, quad 2-input AND	———
U21	7402, quad 2-input NOR	———
U22	7402, quad 2-input NOR	———
U23	75461	———
U24	7408, quad 2-input AND	———
U25	7474, dual "D" flip-flop positive-edge-triggered	AMX3681
U26	9602, dual one-shot re-triggerable	AMX3694
U27	7408, quad 2-input AND	———
U28	7486, quad 2-input EXCLUSIVE-OR	AMX4317
U29	7404, Hex inverter	———
U30	LM339	———
U31	9602, dual one-shot, re-triggerable	AMX3694
U32	75461	———
	JACKS	
J1	Connector - HDR	AJ6728
	RESISTORS	
R1	4.64K, ¼W, 1%	AN0246BEC
R2	4.64K, ¼W, 1%	AN0246BEC
R3	10 ohm, ½W, 5%	AN0063EFB
R4	11K, ¼W, 1%	AN0285BEE
R5	11K, ¼W, 1%	AN0285BEE
R6	11K, ¼W, 1%	AN0285BEE
R7	11K, ¼W, 1%	AN0285BEE
R8	5.11K, ¼W, 1%	AN0253BEE
R9	215 ohm, ¼W, 1%	ARX0146
R10	215 ohm, ¼W, 1%	ARX0146
R11	511 ohm, ¼W, 1%	ARX0151
R12	511 ohm, ¼W, 1%	ARX0151
R13	22.1 ohm, ¼W, 1%	ARX0144
R14	1K, ¼W, 1%	AN0196BEE

SYMBOL	DESCRIPTION	RADIO SHACK PART NUMBER
	RESISTORS (cont'd)	
R15	1K, ¼W, 1%	AN0196BEE
R16	12.1 ohm, ¼W, 1%	ARX0145
R17	10K, ¼W, 1%	AN0281BEE
R18	147 ohm, ¼W,1%	ARX0152
R19	24.9K, ¼W, 1%	AN0313BEC
R20	56.2K, ¼W, 1%	ARX0142
R21	8.25K, ¼W, 1%	ARX0143
R22	56.2K, ¼W, 1%	ARX0142
R23	24.9K, ¼W, 1%	AN0313BEC
R24	150 ohm, 2W, 5%	AN0142EHB
R25	5.11K, ¼W, 1%	AN0253BEE
R26	10 ohm, 1W, 5%	AN0063EGB
R27	51.1K, ¼W, 1%	ARX0148
R28	511 ohm, ¼W, 1%	ARX0151
R29	4.64K, ¼W, 1%	AN0246BEC
R30	T. S.	
R31	T. S.	
R32	T. S.	
R33	7.5K, ¼W, 1%	AN0266BEE
R34	511 ohm, ¼W, 1%	ARX0151
R35	7.5K, ¼W, 1%	AN0266BEE
R36	10K, ¼W, 1%	AN0281BEE
R37	1.1K, ¼W, 1%	AN0198BEE
R38	T. S.	
R39	1K, ¼W, 1%	AN0196BEE
R40	150 ohm, 2W, 5%	AN0142EHB
R41	2.4K, ½W, 5%	AN0219EFB
R42	5.11K, ¼W, 1%	AN0253BEE
R43	5.11K, ¼W, 1%	AN0253BEE
R44	5.11K, ¼W, 1%	AN0253BEE
R45	5.11K, ¼W, 1%	AN0253BEE
R46	5.11K, ¼W, 1%	AN0253BEE
R47	4.64K, ¼W, 1%	AN0246BEC
R48	5.11K, ¼W, 1%	AN0253BEE
R49	5.11K, ¼W, 1%	AN0253BEE
R50	60 ohm, ½W, 5%	AN0545EFB
R51	Not Used	———
↓	↓	↓
R54	Not Used	———
R55		
R56	1K, ¼W, 1%	AN0196BEE
R57	8.66K, ¼W, 1%	ARX0150
R58	10K, ¼W, 1%	AN0281BEE
R59		
R60	5.11K, ¼W, 1%	AN0253BEE
R61	10K, ¼W, 1%	AN0281BEE
R62	100 ohm, ¼W, 1%	AN0132BEE
R63	5.11K, ¼W, 1%	AN0253BEE
R64	511 ohm, ¼W, 1%	ARX0151
R65	511 ohm, ¼W, 1%	ARX0151
R66	20K, ¼W, 1%	AN0306BEE
R67	23.7K, ¼W, 1%	
R68	511 ohm, ¼W, 1%	ARX0151

9404B DISK DRIVE ELECTRICAL PARTS LIST (cont'd)

SYMBOL	DESCRIPTION	RADIO SHACK PART NUMBER
	RESISTORS (cont'd)	
R69	Not Used	———
↓	↓	↓
R74	Not Used	———
R75	3.16K, ¼W, 10%	AN0229FEB
R76	1.96K, ¼W, 1%	ARX0147
R77	Not Used	———
R78	10K, ¼W, 1%	AN0281BEE
R79	1K, ¼W, 1%	AN0196BEE
R80	10K, ¼W, 1%	AN0281BEE
R81	150K, 2W, 5%	AN0142EHB
R82	5.11K, ¼W, 1%	AN0253BEE
R83	Not Used	———
R84	10K, ¼W, 1%	AN0281BEE
R85	51.1K, ¼W, 1%	ARX0148
R86	31.6K, ¼W, 1%	ARX0149
R87	Not Used	———
R88	511 ohm, ¼W, 1%	ARX0151
R89	5.11K, ¼W, 1%	AN0253BEE
R90	5.11K, ¼W, 1%	AN0253BEE
R91	Not Used	———
	RESISTORS (cont'd)	
R92	24.9K, ¼W, 1%	AN0313BEC
R93	5.11K, ¼W, 1%	AN0253BEE
R94	102 ohm, ¼W, 1%	AN0133BEE
R95	1K, ¼W, 1%	AN0196BEE
R96	909 ohm, ¼W, 1%	AN0191BEB
RM1	Resistor Pak 220/330 ohm	ARX0141
	SWITCH	
S1	rocker, 8-position	AS0964
	TRANSISTORS	
VR1	357DL, +12V regulator	AS0964
Q1	7826, 2N2907A	AMX3679
Q2	7821, TP125	———
Q3	7817, TP120	AMX4195
Q4	7817, TP120	AMX4195
Q5	7817, TP120	AMX4195

SECTION XV

AA11100 POWER SUPPLY

A. FUNCTIONAL SPECIFICATIONS

The power supply for the TRS-80 Model II Disk Expansion System is a 60 watt switching power supply. Connections to the power supply module are made via a standard feed-through barrier terminal block. Each circuit of the terminal block is rated 230 VAC @ 10 amps.

In theory, the power supply rectifies the AC line to DC then chops it at 20 kHz. The chopped DC voltage is then transformed to the required output voltages and rectified to low voltage isolated DC. Feedback loops are provided for voltage regulation and over current protection.

The power supply may be jumper selected for either of the following ratings (see Figure 1):

Vin - 95 to 135VAC @ 47 to 63Hz input frequency
or - 190 to 270VAC @ 47 to 63Hz input frequency

The power supply module can withstand the following maximum ratings:

Vin (AC continuous) - 140V input select 115V
or - 280V input select 230V

Short Circuit, any output - indefinite

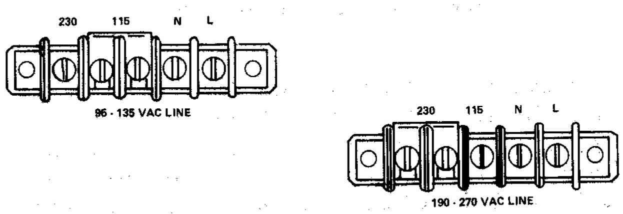


Figure 1. Line Voltage Selection

B. TROUBLESHOOTING

1. Equipment for Test Set-Up

a. Isolation Transformer (minimum of 500 VA rating) –

> ***CAUTION***
>
> Dangerously high voltages are present in this power supply. For the safety of the individual doing the testing, please use an isolation transformer. The 500 VA rating is needed to keep the AC waveform from being clipped off at the peaks. These power supplies have peak charging capacitors and draw full power at the peak of the AC waveform.

b. 0-140V Variable Transformer (Variac) – Used to vary input voltage. Recommend 10 amp, 1.4 KVA rating, minimum.

c. Voltmeter – Need to measure DC voltages to 50 VDC and AC voltages to 200 VAC. Recommend two digital multimeters.

d. Oscilloscope – Need X10 and X100 probes.

e. Load board with Connectors – See Table 1 for values of loads required. The entry on the table for Safe Load Power is the minimum power ratings for the load resistors used.

NOTE: Because of its design, this power supply must have a load present or damaging oscillations may result. **Never test the power supply without a suitable load!**

f Ohmmeter

2. Set-Up Procedure

Set-up as shown in Figure 2. You will want to monitor the input voltage and the output voltage of the regulated bus, which is the +5 output, with DVM's. Also monitor the +5 output with the oscilloscope using 50mv/div sensitivity. The DVM monitoring the +5 output can also be used to check the other outputs. See text of section III for test points within the power supply.

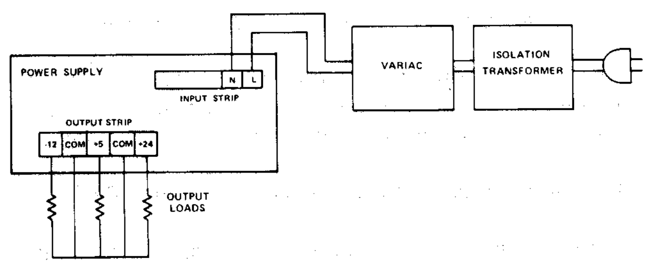


Figure 2. Test Set-up

3. Visual Inspection

Check power supply for any broken, burned, or obviously damaged components. Visually check fuse, if any question check with ohmmeter.

4. Start-Up

Load power supply with minimum load as specified in Table 1. Bring up power slowly with Variable Transformer while monitoring the +5 output with the oscilloscope and DVM. Supply should start with approximately 40-60 VAC applied, and should regulate when 95 VAC is reached. If output has reached 5 volts, do a performance test as shown in section D. If there is no output, refer to section C.

Table 1. LOAD BOARD VALUES

OUTPUT	MIN LOAD	LOAD R	SAFE LOAD POWER	MAX LOAD	LOAD R	SAFE LOAD POWER
+5	0.75A	6.67 ohm	8W	3A	1.67 ohm	30W
+24	0	0	0	1.7A	14.12 ohm	80W
-12	0.042A	286 ohm	1W	0.17A	70.6 ohm	4W

5. Disassembly

Top and bottom covers are fastened by six machine screws per cover. With these covers removed, both sides of the main PCB are exposed. This should be sufficient for most repairs. If needed, the side PCB can be removed by de-soldering a row of 14 points located ½-inch from the side of the main PCB nearest to the rectifier heat sink. The rectifier heat sink is the side of the chassis behind the side PCB.

C. NO OUTPUT

1. Check Fuse

If fuse is blown, replace it but do not apply power until cause of failure is found.

2. Preliminary Check on Major Primary Components

Check diode bridge (BR1), power transistor (Q1), catch diode (D3), and diode D1. Diodes D3 and D1 are rectifiers which attach to the power transistor heat sink.

3. Preliminary Check on Major Secondary Components

Using an ohmmeter from an output that is common to each output and with output loads disconnected, check for shorted rectifiers or capacitors. If the +5 is shorted, also check crowbar SCR (SCR 1) and zener diode (Z1).

4. Check for B+

Set up power supply and attach X100 scope probe ground to the negative terminal of the large input capacitor nearest to the control module. Slowly turn up power and check for B+ on the metal plate riveted to the power transistor heat sink. With input at 95 VAC, this point should read 250-300 VDC. If this is not correct, check fuse, BR1, and if necessary, TM1, TM2, D1, and D17. Also check input capacitors C5 and C6 and see that the connections from the barrier strip to the PCB are good.

5. Check Q1 Waveforms

Using X100 probe on case of TO-3 package of Q1, check collector waveform. Transistor should be switching. The correct waveform is shown in Figure 3. If switching is not present, check for shorted junctions on Q1. If OK, check the base waveform.

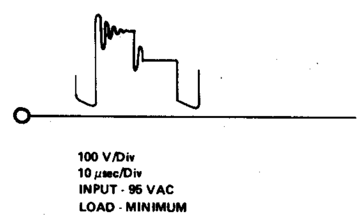


Figure 3. Q1 Collector Waveforms

The base of Q1 (looking under the PCB) is the pin from the center of Q1, closest to the PCB corner. The correct waveform is shown in Figure 4. If the waveform is not there, check for clock pulses which will show as spikes of approximately 2 volts magnitude every 50 µsec. If these spikes are not there, then control module should be replaced, especially if no other component failures can be found.

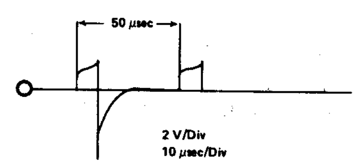


Figure 4. Q1 Base Waveforms

D. PERFORMANCE TEST

Each of these test conditions should be set-up and noted to be within the limits specified in Table 2.

Test	Input	+5 Load	+24 Load	-12 Load
1	95VAC	Max	Max	Max
2	135VAC	Max	Max	Max
3	*135VAC	Max	Max	Max
4	135VAC	Min	Min	Min
5	95VAC	Min	Min	Min

*On test 3, input voltage should be varied over full range to search for instability after correct outputs are noted at 135 VAC.

TABLE 2. VOLTAGE AND RIPPLE SPECIFICATIONS

OUTPUT	MIN	MAX	NO LOAD	RIPPLE
+5	4.90V	5.10V	-	50mV P-P
+24	21.20V	26.40V	30.0V	250mV P-P
-12	-11.40V	-12.60V	-	50mV P-P

OPERATING CHARACTERISTICS

	MIN	TYP	MAX	UNITS
Vin Range				
Input Select 115V	95	115	135	VAC
Input Select 230V	190	230	270	VAC
Line Frequency	47	50/60	63	Hz
Output Voltages VO1	21.60	24.00	30.00	V
VO2	4.90	500	510	V
VO3	-11.40	-12.00	-12.60	V
Output Current IO1	0	1.3	1.7	A
IO2	0.75	2.40	3.00	A
IO3	0	0.12	0.17	A
VCB +5V Crowbar Fire	594	----	7.00	V
OCP, Current Limit ICL1	2.00	2.50	3.50	A
ICL2	4.00	5.00	7.00	A
Ripple Voltages VRIP1	----	----	100	mV
VRIP2	----	----	50	mV
VRIP3	----	----	50	mV
Efficiency	70	----	----	%
Hold Up Time				
Full Load, Lo Line	10	----	----	mSec
Full Load, Nom Line	16	----	----	mSec
Insulation				
Input to GND	50	----	----	M ohms
Input to Outputs	50	----	----	M ohms
Output to GND	50	----	----	M ohms
Isolation				
Input to GND	4.24	----	----	KVDC
Input to Outputs	4.24	---	----	KVDC
Transient Reponse				
@ Load Change on Any Output From 25% to 75% and 75% to 25% Within Regulation Limit	----	----	500	μSec

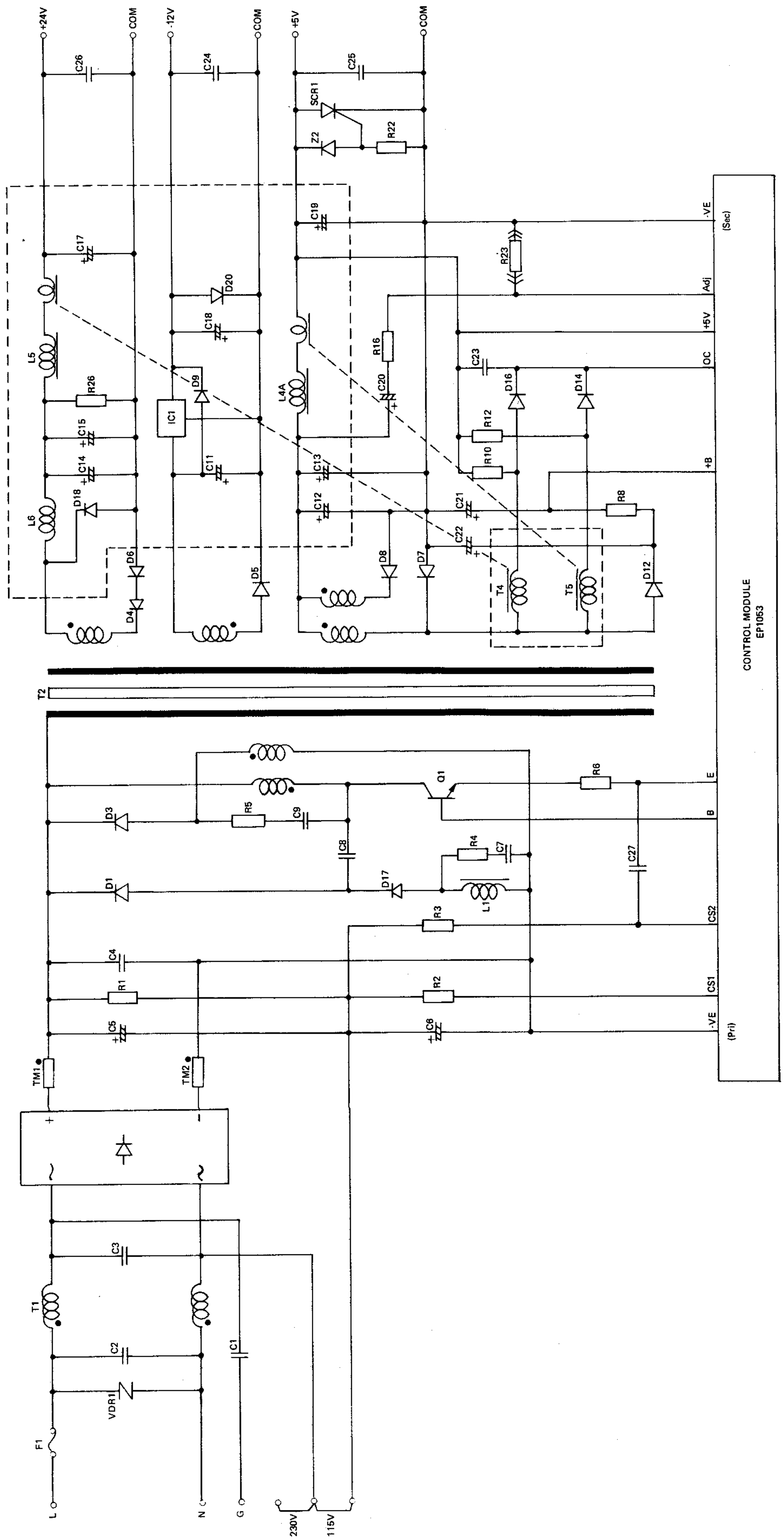


Figure 5. AA11100 Power Supply Schematic

SECTION XVI

ILLUSTRATED PARTS BREAKDOWN

CASE ASSEMBLY PARTS LIST

REF NUMBER	DESCRIPTION	MANUFACTURER'S PART NUMBER	RADIO SHACK PART NUMBER
1	Case, upper	8719029	AZ5196
2	Case, bottom	8719028	AZ5195
3	Screw, 8-32 x ½" (12.7mm), PH (2)	8569050	AHD1553
4	Rear Panel	8729016	AZ5223
5	Plate Adapter	8729017	AZ5224
6	Cable, Disk Bus	8709055	AW2423
7	Cable, Parallel I/O	8709050	AW2422
8	Cable, Serial I/O	8709056	AW2424
9	Connector, Power Cord	8519013	AJ6761
10	Fuse Holder w/hardware	8519048	AHF1161
10	Fuse, 2A	8479001	AHF1160
*10	Fuse, 1A	8479002	
11	Washer, flat, #4 (6)	8589002	AHD8500
12	Washer, lock, #4 (10)	8589021	AHD8518
13	Hex Nut, #4 (10)	8579012	AHD7166
14	Screw, 8-32 x ½" (12.7mm), PH (8)	8569050	AHD1553
	†Washer, flat, #8 (8)	8589016	AHD8513
	†Washer, lock, #8 (8)	8589013	AHD8511
	†Hex Nut, #8 (8)	8579013	AHD7167
15	Screw, 4-40 x ½" (12.7mm), PH (10)	8569033	AHD1542
16	Screw, 6 x ¼" (6.35mm) thread-forming (4)	8569040	AHD1547
17	Washer, flat, #8 (2)	8589016	AHD8513
	†Screw, 8 x 3/8" (9.5mm) SL/Hex/Wash (5)	8569030	AHD1539
	†Feet, black, polyethleene (4)	8599072	AHB9436
	†Screw, 6 x 3/8" (9.5mm), Plastite (4)	8569047	AHD1552

*For overseas models only.

†Not shown on illustration.

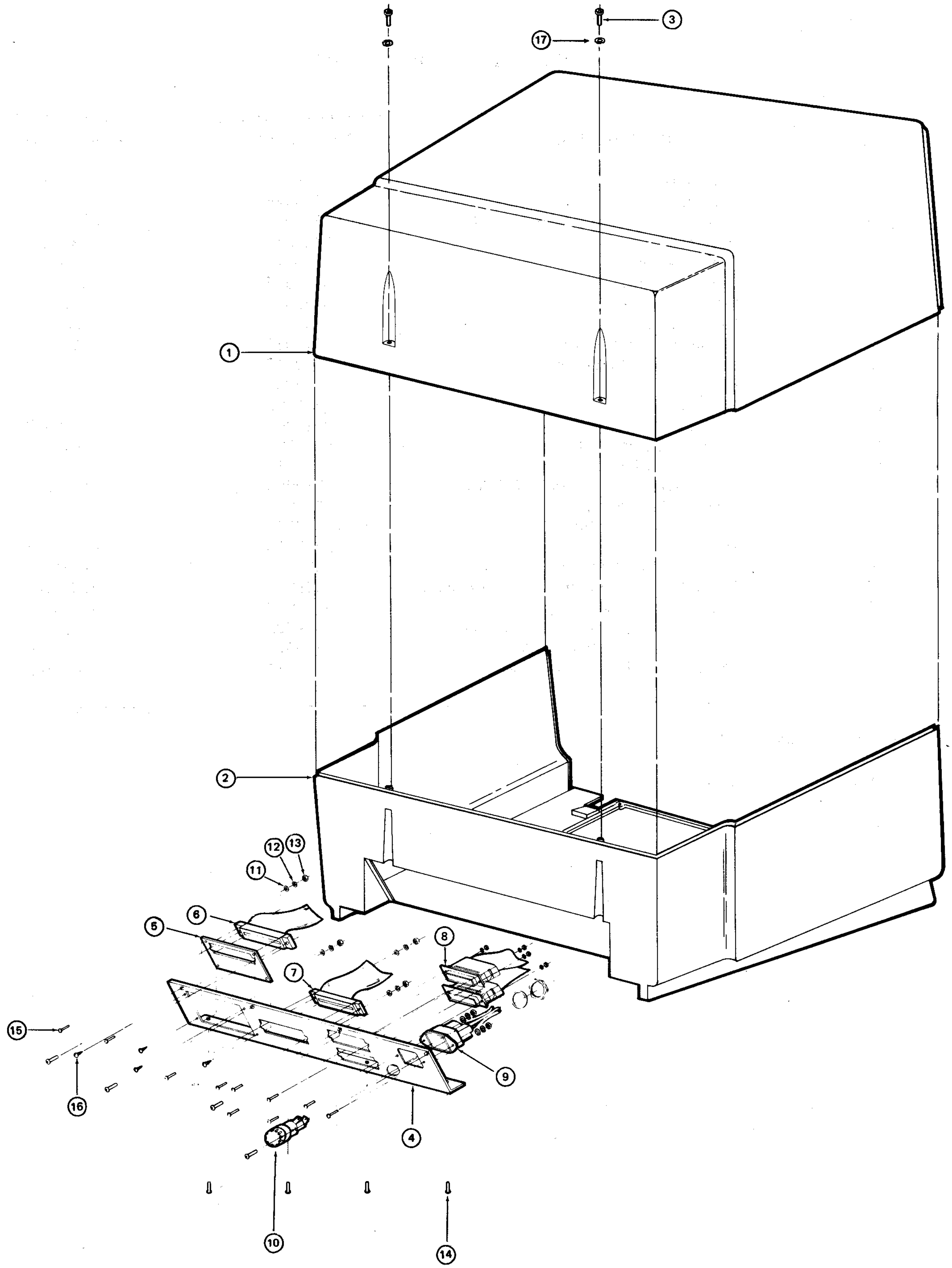


Figure 1. Case Assembly

CHASSIS ASSEMBLY PARTS LIST

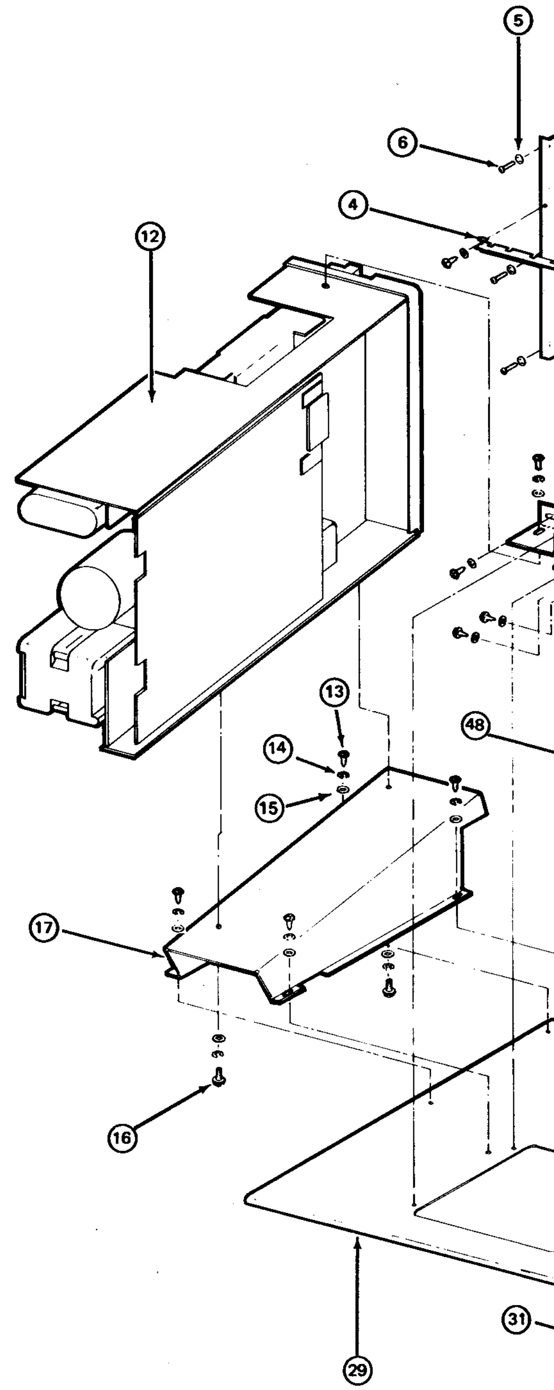
REF. NUMBER	DESCRIPTION	MANUFACTURER'S PART NUMBER	RADIO SHACK PART NUMBER
1	Motherboard Assy.	8893430	AXX0500
2	Bracket, right side	8729011	ART2682
3	Bracket, left side	8729015	ART2686
4	Card Guide Support	9729013	ART2684
5	Washer, flat, #4 (6)	8589002	AHD8500
6	Screw, 4-32 x ½" (12.7mm) (6)	8569033	AHD1542
7	Washer, lock, #4 (6)	8589021	AHD8518
8	Nut, Hex, #4 (6)	8579012	AHD7166
9	Screw, 6 x ¼" (5.35mm), thread-forming (4)	8569040	AHD1547
10	Screw, 8 x 3/8" (9.5mm) (2)	8569030	AHD1539
11	Washer, flat, #8 (2)	8589016	AHD8513
12	Disk Drive, SA-800, 60Hz	8893536	AXX5002
*12	Disk Drive, SA-800, 50Hz	8893582	
13	Screw, 8 x 3/8" (9.5mm), zinc, thread-forming (4)	8569054	AHD1555
14	Washer, lock, #8 (7)	8589013	AHD8511
15	Washer, flat, #8 (7)	8589016	AHD8513
16	Screw, 8 x 3/8" (9.5mm) (3)	8569030	AHD1539
17	Bracket, Disk	8729009	ART2680
18	Screw, 8 x ½" (12.7mm), phillips (2)	8569056	AHD1556
19	Washer, flat, #8 (4)	8589016	AHD8513
20	Switch, momentary, N/O	8489016	AS9125
21	Screw, 4 x ¼" (6.35mm), phillips (4)	8569032	AHD1541
22	Switch, rocker, 4A	8489017	AS9126
23	LED, red	8469004	AL1102
24	LED Mounting	8559001	ART1951
25	Bezel, front	8719030	AZ5197
26	Screw, 8 x 3/8" (9.5mm), zinc, thread-forming (2)	8569054	AHD1555
27	Washer, lock, #8 (4)	8589013	AHD8511
28	Nut, Hex, #8 (4)	8579013	AHD7167
29	Bracket, Baseplate	8729006	ART2677
30	Fan	8790505	AXX5008
31	Washer, lock, #6 (4)	8589018	AHD8515
32	Screw, 6-32 x 2" (50.8mm) (4)	8569052	AHD8499
33	Nut, Hex, #6 (4)	8579014	AHD7168
34	Washer, flat, #6 (4)	8589017	AHD8514
35	Power Supply w/Bracket	8893523	AXX6003
36	Video, PCB assy.	84V25561A93	AXX0312
37	Screw, 4-40 x ¼" (6.35mm), phillips (4)	8569031	AHD1540
38	Washer, lock, #4 (4)	8589021	AHD8518
39	Washer, flat ¼" (4)	8589015	AHD8512
40	Screw, 8 x 3/8" (9.5mm), zinc, thread-forming (3)	8569054	AHD1555
41	Screw, 4-32 x ½" (12.7mm) (2)	8569033	AHD1542
42	Washer, lock, #4 (2)	8589021	AHD8518
43	CRT, 12"	96R2500A15	AXX8002
44	Screw, 8-32 x ½" (12.7mm) (4)	8569050	AHD1553
	†Washer, flat, #4 (2)	8589002	AHD8500
	†Nut, Hex, #4 (2)	8579012	AHD7166
45	Washer, flat #8 (4)	8589016	AHD8513

CHASSIS ASSEMBLY PARTS LIST (cont'd)

REF. NUMBER	DESCRIPTION	MANUFACTURER'S PART NUMBER	RADIO SHACK PART NUMBER
46	Washer, lock, #10 (4)	8589020	AHD8517
47	Bracket, Bezel, lower	8729032	AHB9449
48	Bracket, Video Mounting (2)	8729010	ART2682
49	Bracket, Bezel Mounting	8729031	ART2719
50	Screw, 8 x 3/8" (9.5mm), zinc, thread-forming (10)	8569054	AHD1555
51	Washer, flat, #8 (10)	8589016	AHD8513
52	Pot, Contrast	8260150	AP7023
53	Pot, Brightness	8260450	AP7024
	†Screw, 8-32 x 3/8" (9.5mm) (4)	8569030	AHD1539

*For overseas models only.

†Not shown on illustration.



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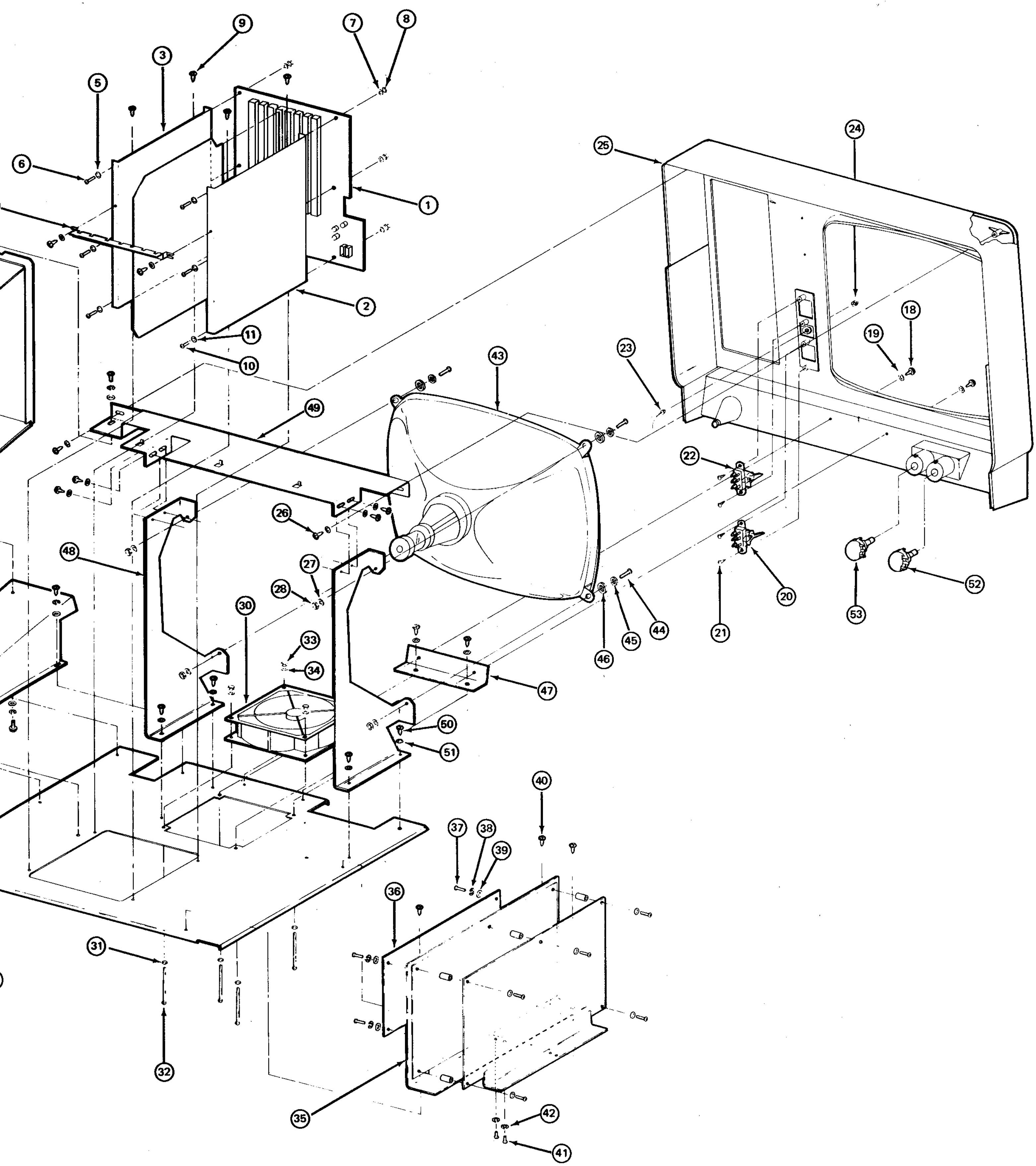
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SECTION XVII

APPENDIXES

LIMITED WARRANTY

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